

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled

UMA:UMA platform installed

OPS:Optimus

HR:Huron River

CR:Chief River

V: V-Series installed

緯創資通

Wistron Corporation

21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title

Cover Page

Size
A4

Document Number

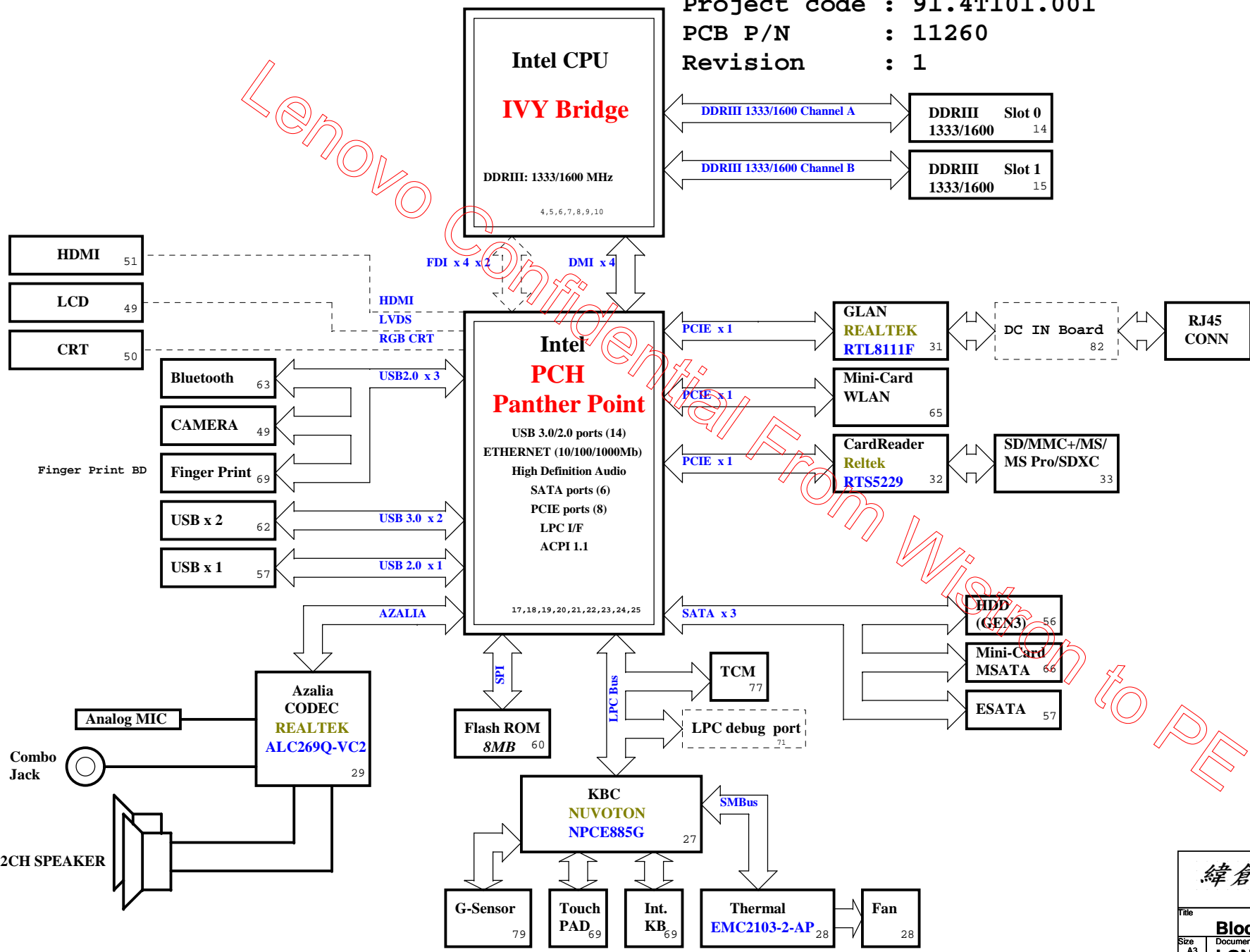
LGN-1

Rev
1

Date: Wednesday, February 15, 2012 Sheet 1 of 103

Block Diagram
(UMA)

Project code : 91.4TI01.001
PCB P/N : 11260
Revision : 1



SYSTEM DC/DC TPS51461 48		CPU DC/DC TPS51640 42~44	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
5V_S5	VCCSA	DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51219 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51225 41	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC RT8207 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC TPS51640 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

INPUTS	OUTPUTS

TI CHARGER BQ24737 40	
INPUTS	OUTPUTS
AD_JK	BT+

SYSTEM DC/DC RT9018B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

INPUTS	OUTPUTS

LDO RT8207 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER	
L1:Top	L5:GND
L2:VCC	L6:Bottom
L3:Signal	
L4:Signal	

PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor (CRB has it pulled up with 1-kohm no-stuff resistor). Disable Danbury: Leave floating (internal pull-down).
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to 1: Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port 0:	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA 0D75V_S0 VCC_CORE VOS_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_S3BX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV
Device		Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA SMML_CLK/SMML_DATA
PCH SMBus SO-DIMM (SPD) SO-DIMM (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

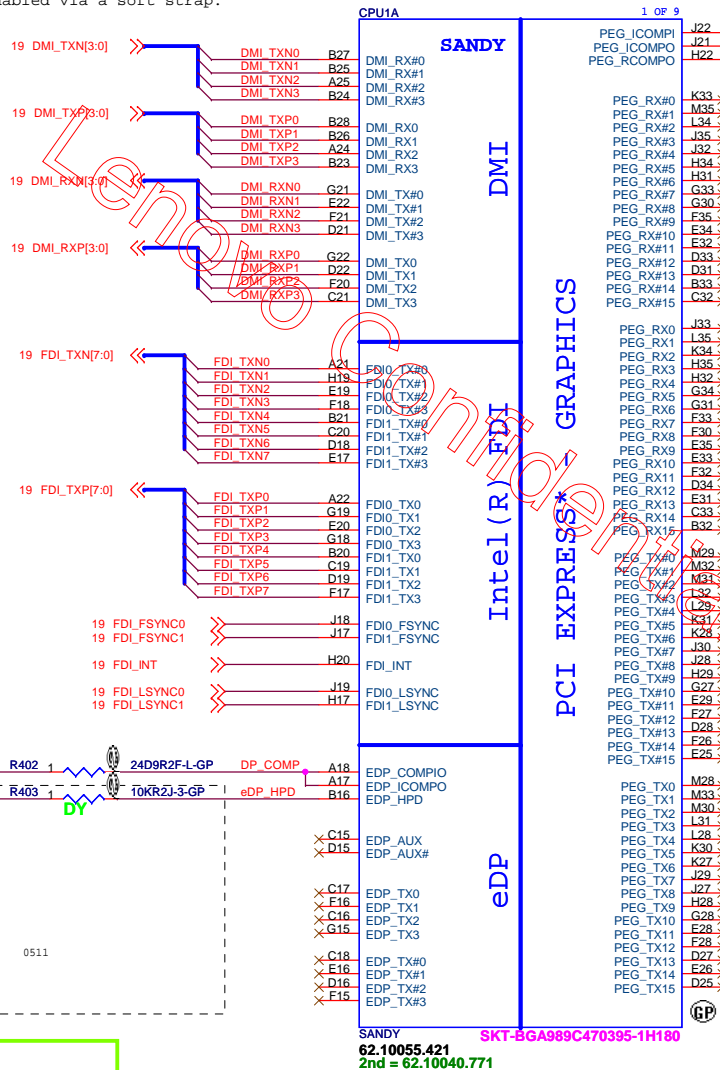
Title		
Table of Content		
Size	Document Number	Rev
A3	LGN-1	1
Date: Wednesday, February 15, 2012		
Sheet	3	of 103

SSID = CPU

01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

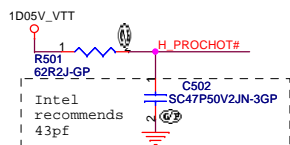
NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

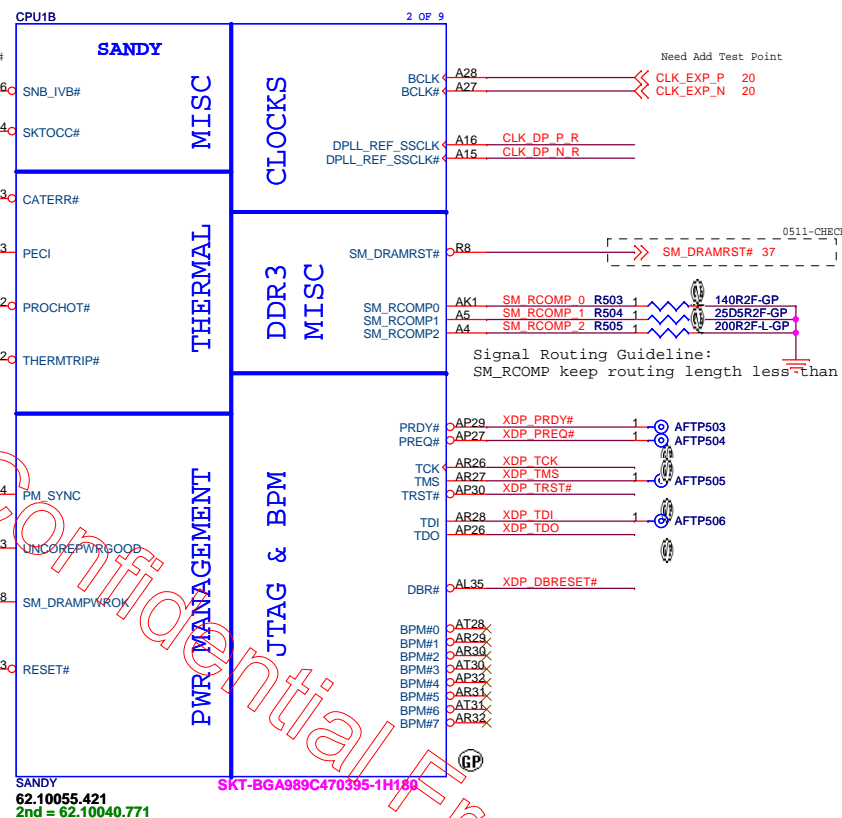
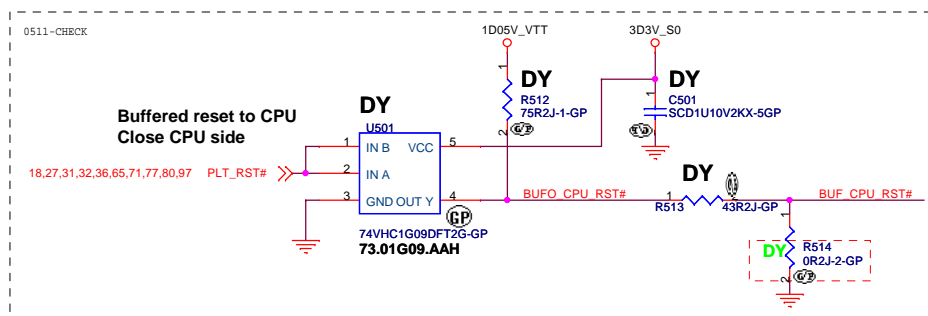
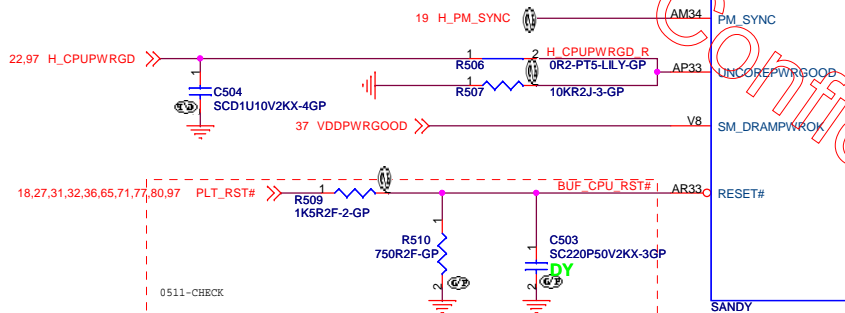
File		CPU (PCIE/DMI/FDI)	
Size	A3	Document Number	Rev 1
LGN-1			
Date:	Wednesday, March 21, 2012	Sheet	4 of 103

SSID = CPU⁵

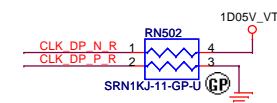


Connect EC to PROCHOT# through inverting OD buffer.

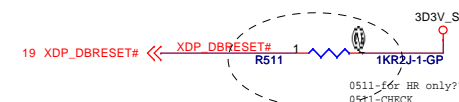
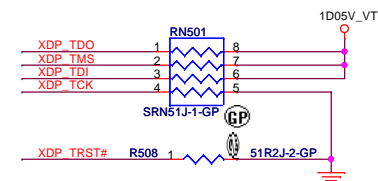
If PROCHOT# is not used, then it must be terminated with a 68ohm $\pm 5\%$ pull-up resistor to VTT.



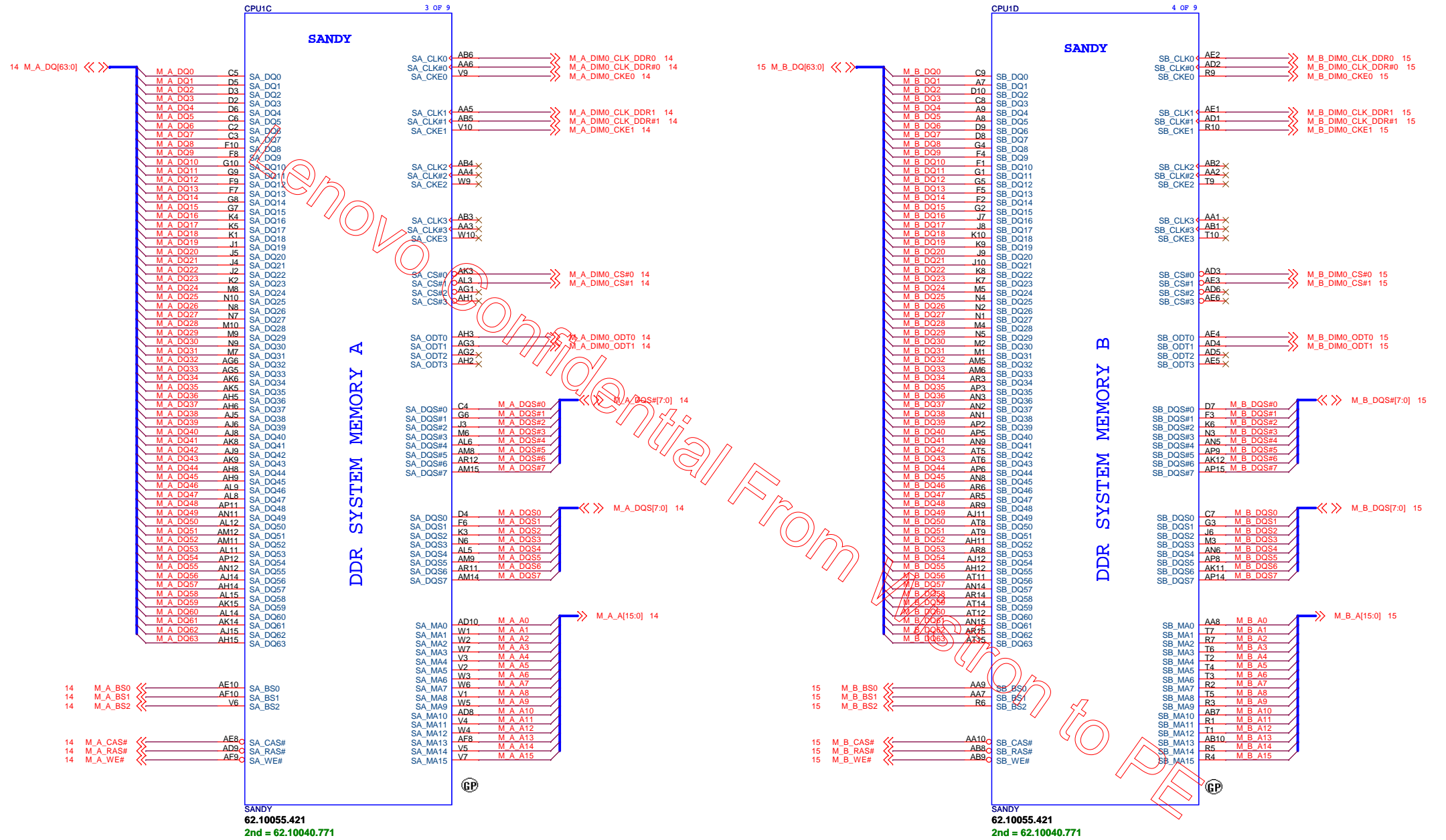
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistor power (~15 mW) may be
wasted.



In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils wide trace for routing less than 500 mils, or 20-mils wide trace for routing between 500 mils and 1000 mils. Keep 20-mils spacing to any other signals in order to minimize crosstalk.



SSID = CPU

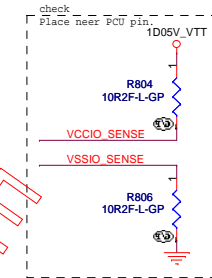
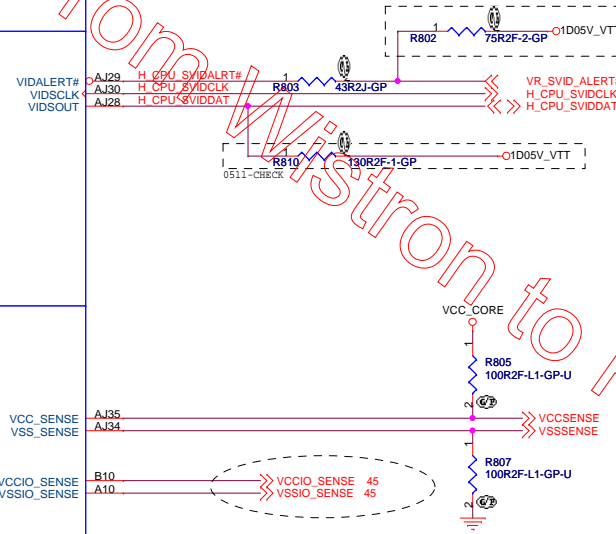
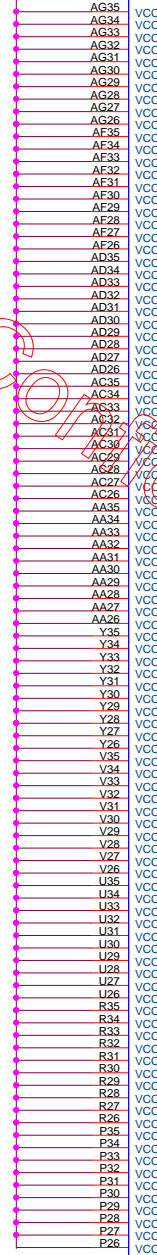


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (DDR)	
Size			LGN-1	
Date: Wednesday, March 21, 2012			Sheet 6 of 103	

SENSE LINES

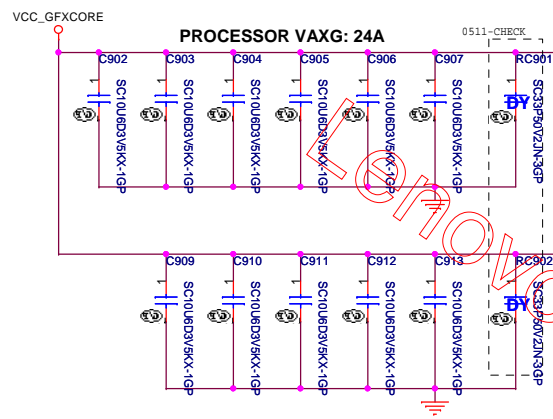


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (VCC CORE)			
Size	Document Number	Rev	
Custom	LGN-1	1	
Date:	Wednesday, March 21, 2012	Sheet 8 of	103

CHECK CAP

0511-CHECK CAP



PROCESSOR VAXG: 24A

0511-CHECK



VCCPLL: 1.2A

VCC1R8B CPU

- CPU1G 7 OF 9
- AT24 VAXG
 - AT23 VAXG
 - AT21 VAXG
 - AT20 VAXG
 - AT18 VAXG
 - AT17 VAXG
 - AR24 VAXG
 - AR23 VAXG
 - AR21 VAXG
 - AR20 VAXG
 - AR18 VAXG
 - AR17 VAXG
 - AP24 VAXG
 - AP23 VAXG
 - AP21 VAXG
 - AP20 VAXG
 - AP18 VAXG
 - AP17 VAXG
 - AN24 VAXG
 - AN23 VAXG
 - AN21 VAXG
 - AN20 VAXG
 - AN18 VAXG
 - AN17 VAXG
 - AM24 VAXG
 - AM23 VAXG
 - AM21 VAXG
 - AM20 VAXG
 - AM18 VAXG
 - AM17 VAXG
 - AL24 VAXG
 - AL23 VAXG
 - AL21 VAXG
 - AL20 VAXG
 - AL18 VAXG
 - AL17 VAXG
 - AK24 VAXG
 - AK23 VAXG
 - AK21 VAXG
 - AK20 VAXG
 - AK18 VAXG
 - AK17 VAXG
 - AJ24 VAXG
 - AJ23 VAXG
 - AJ21 VAXG
 - AJ20 VAXG
 - AJ18 VAXG
 - AJ17 VAXG
 - AH24 VAXG
 - AH23 VAXG
 - AH21 VAXG
 - AH20 VAXG
 - AH18 VAXG
 - AH17 VAXG

POWER

SANDY

SENSE LINES

VREF

DDR3 1.5V RAILS

SA RAIL

MISC

1.8V RAIL

SANDY
62.10055.421
2nd = 62.10040.771

BOM Control

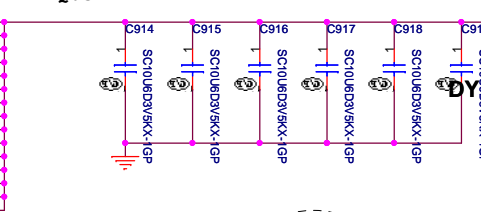
	RN901
HR	10K ohm
CRV	1K ohm
	66.10236.04L

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

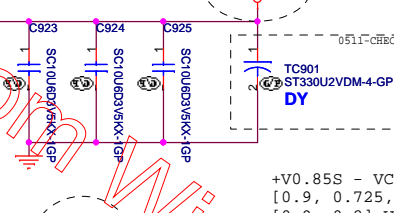
+V_SM_VREF_CNT should have 10 mil trace width

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VDDQ: 5A

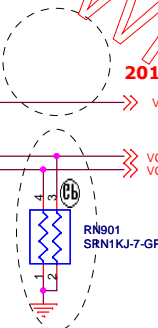


VCCA: 6A

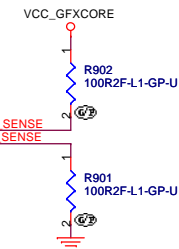


+V0.85S - VCCSA - System Agent rail voltage can be [0.9, 0.725, 0.8, 0.675] V for IVB [0.9, 0.8] V for SNB

20110103



check place



check Cap.

1D5V_S0

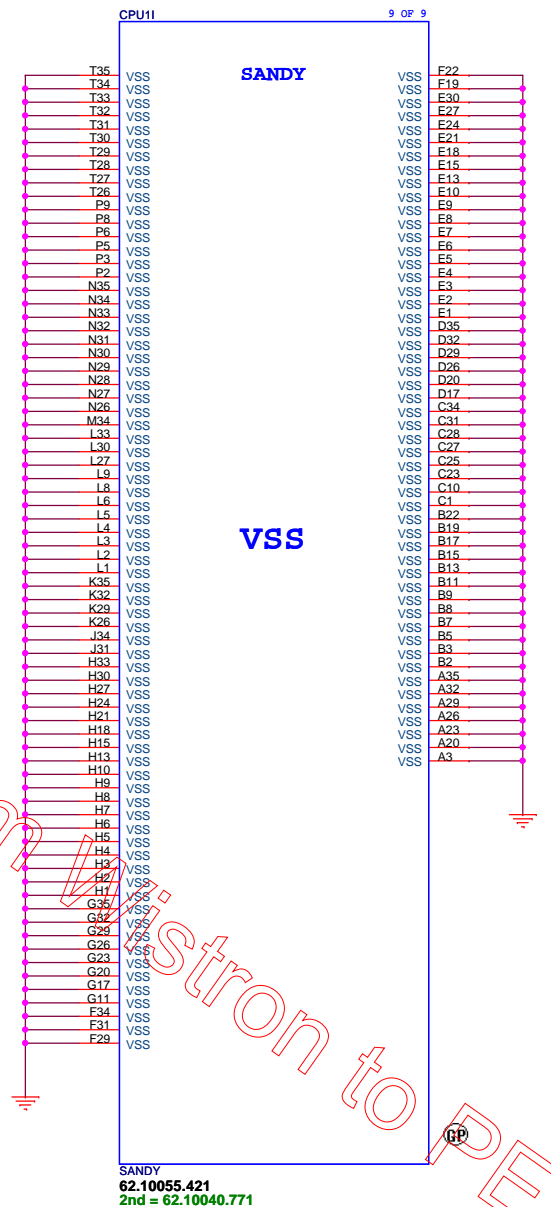
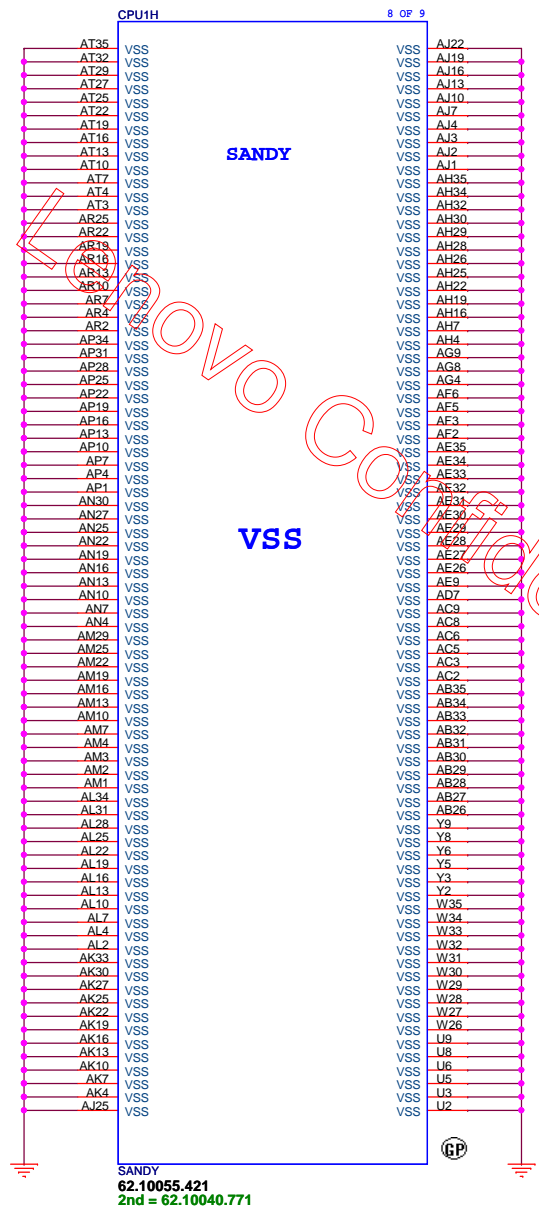
R904
0R0306-PAD-GP

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (VCC GFXCORE)		
Size	Document Number	Rev	
A3	LGN-1	1	
Date:	Wednesday, March 21, 2012	Sheet	9 of 103

SSID = CPU



D

C

B

A

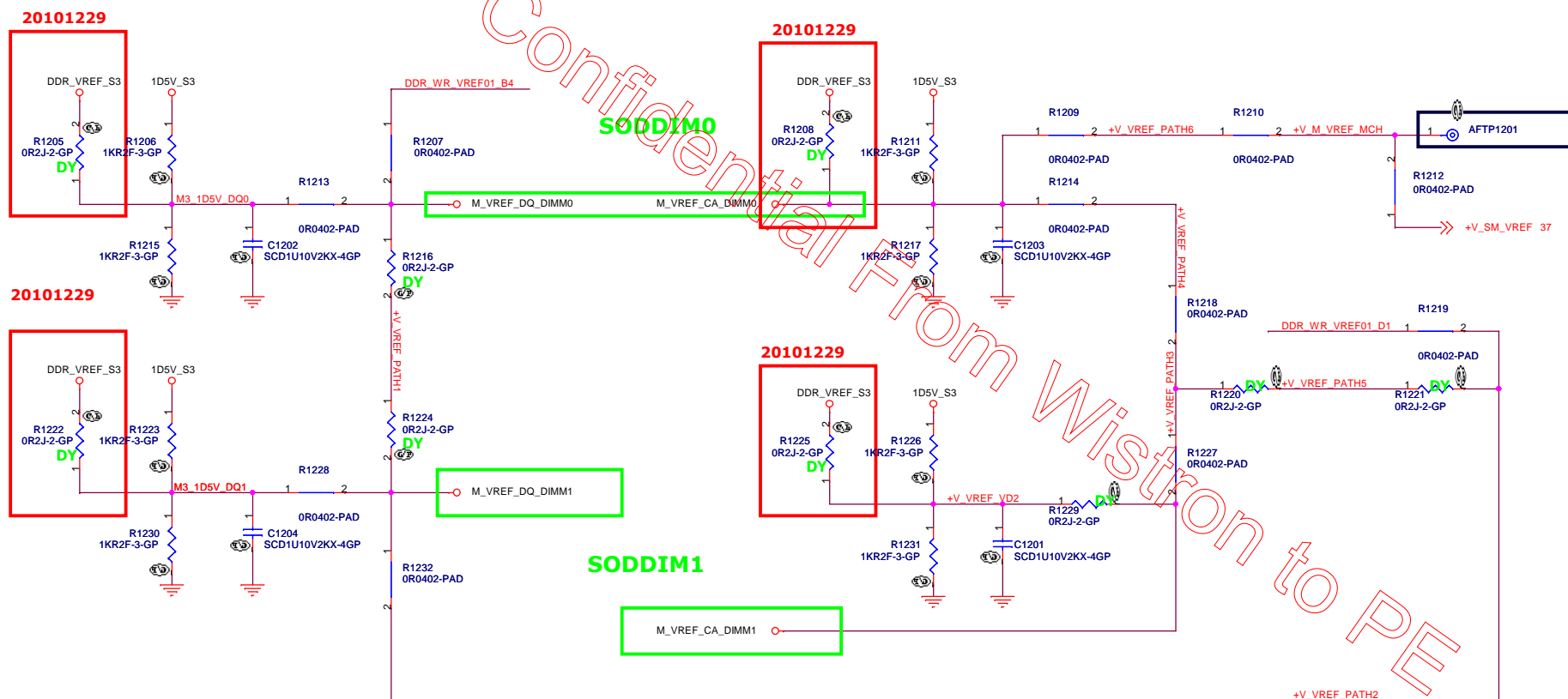
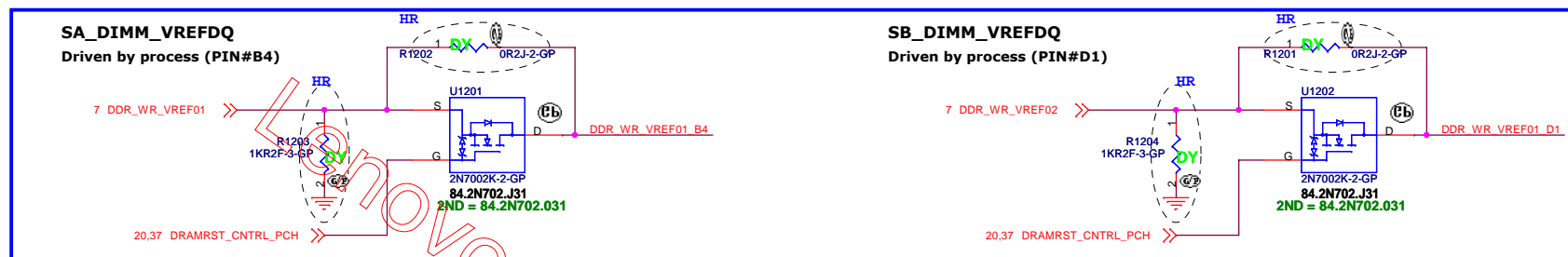
Lenovo Confidential From Wistron to PE

BLANK

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</div>		
Title <Title>		
Size A4	Document Number LGN-1	Rev 1
Date: Wednesday, February 15, 2012	Sheet 11	of 103

For CRV:

CAD Note: All VREF traces should have 20:20 mil trace geometry



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

M3

Size

Document Number

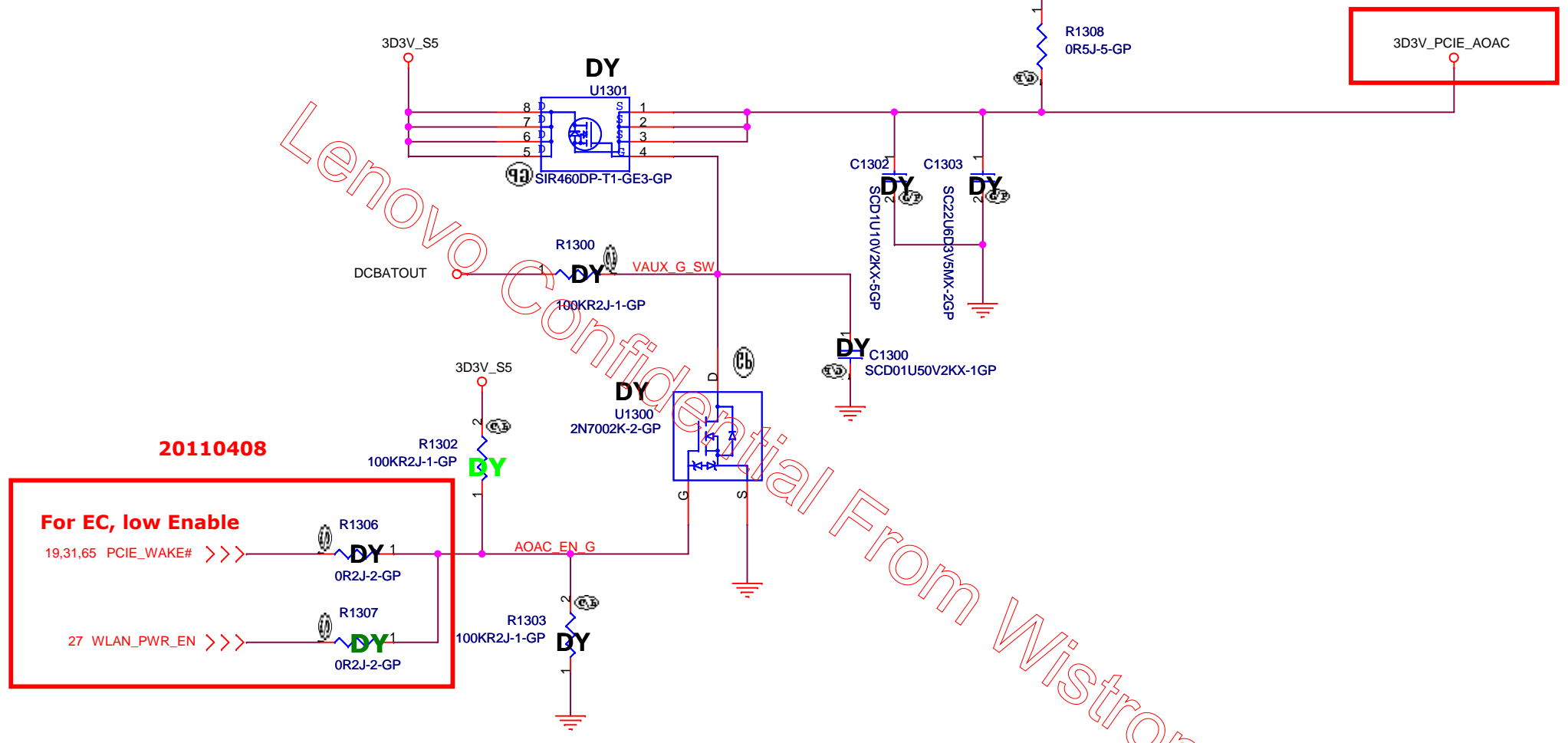
LGN-1

Rev

Date: Wednesday, March 21, 2012

Sheet 12 of 103

3D3V_PCIE_AOAC tie to I/O board WLAN, WWAN



20110408

For EC, low Enable

19,31,65 PCIE_WAKE# >>>

R1306
0R2J-2-GP

27 WLAN_PWR_EN >>>

R1307
0R2J-2-GP

<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AOAC

Size
A4

Document Number

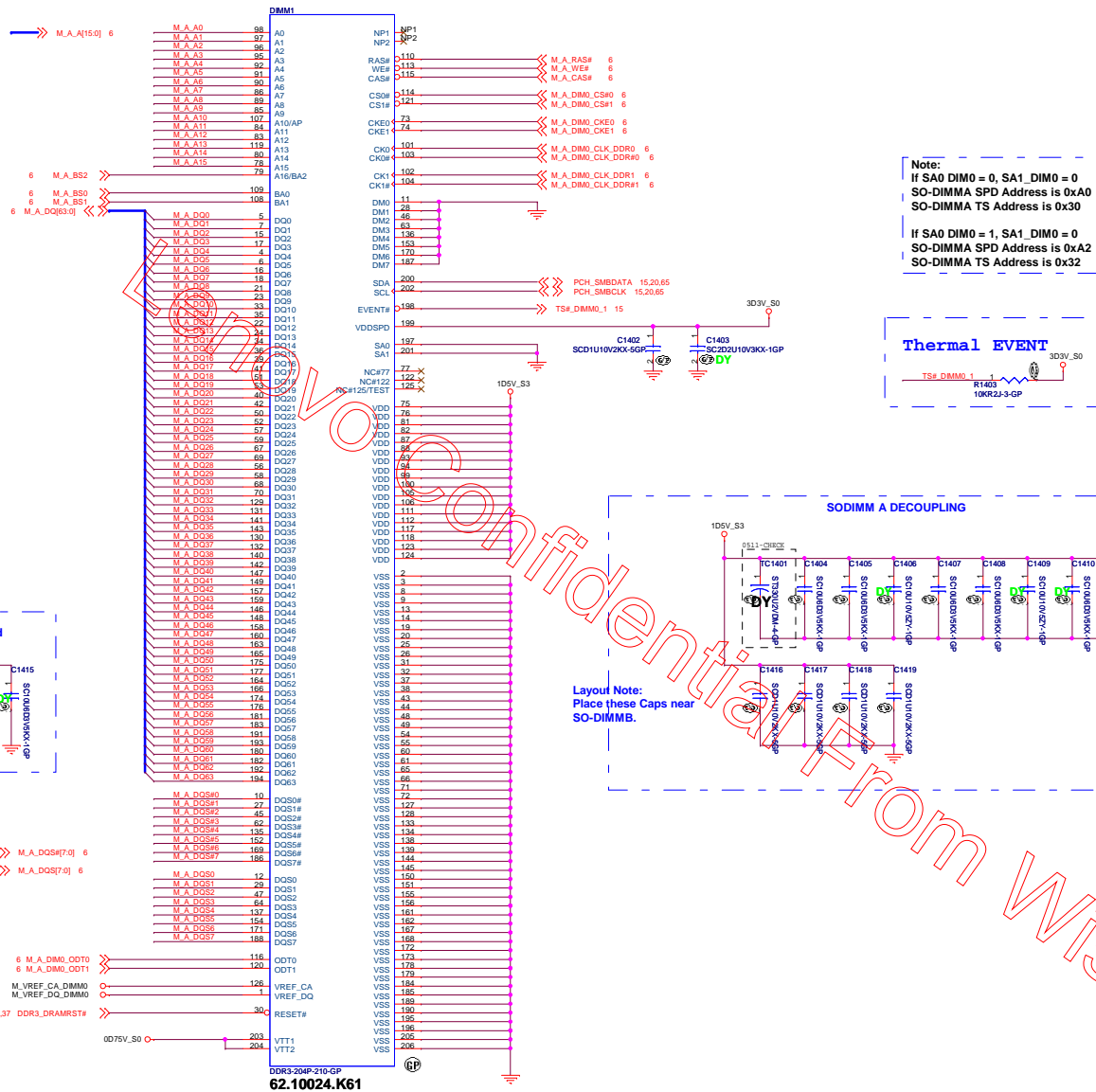
LGN-1

Rev
1

Date: Wednesday, March 21, 2012

Sheet 13 of 103

SSID = MEMORY

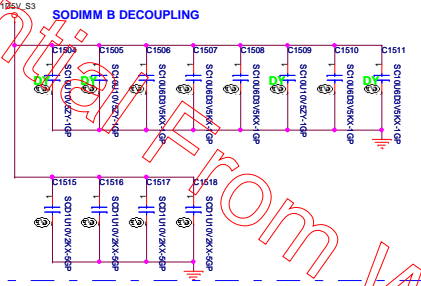
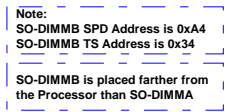


Place these caps close to VTT1 and VTT2.

0D75V_S0

C1501 C1512 C1513 C1514

DY SCU0002X-6P



Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DDR3-SODIMM2			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 16 of	103

L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display

Close to PCH
 Close to PCH and keep 20mil
 away from other signal.

Close to PCH

Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k $\pm 0.5\%$. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

DDI Port B Detect: (SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

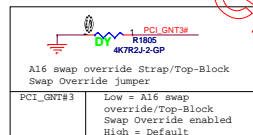
HDMI

PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_0[P]	TMDSB_DATA2#
	DDPB_0[N]	TMDSB_DATA2#
	DDPB_1[P]	TMDSB_DATA1#
	DDPB_1[N]	TMDSB_DATA1#
	DDPB_2[P]	TMDSB_DATA0#
	DDPB_2[N]	TMDSB_DATA0#
	DDPB_3[P]	TMDSB_CLK
	DDPB_3[N]	TMDSB_CLK#
	DDPB_AUXN	NA
	DDPB_HPDP	HDMI_B_HPDP
	SDVO_CTRLCLK	HDMI_B_CTRLCLK
	SDVO_CTRLDATA	HDMI_B_CTRLDATA

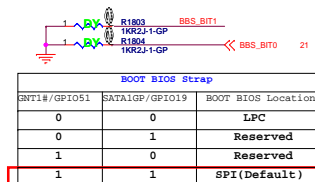
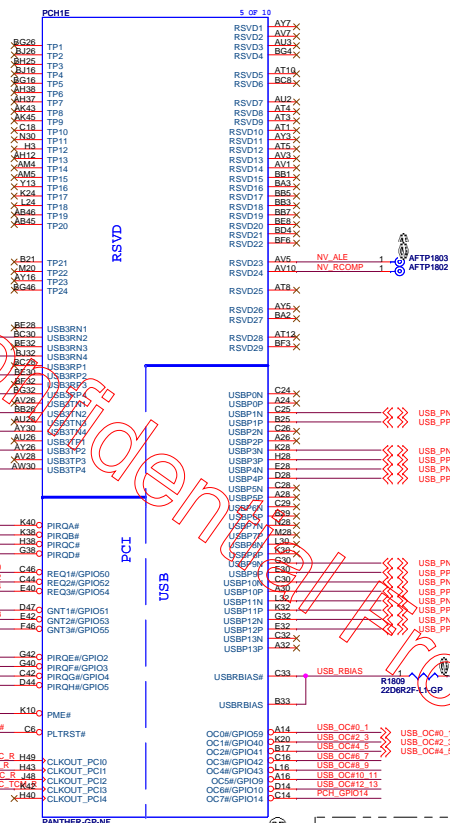
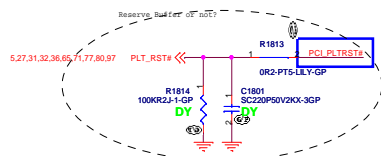
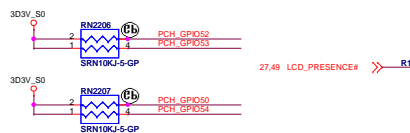
<Variant Name>

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH : LVDS/CRT/DDI		
Size	Document Number	Rev
A3	LGN-1	1
Date: Wednesday, March 21, 2012		
Sheet 17 of 103		



```
62 USB3_RX1_N >>
62 USB3_RX3_N >>
62 USB3_RX1_P >>
62 USB3_RX3_P >>
62 USB3_TX1_N <<
62 USB3_TX3_N <<
62 USB3_TX1_P <<
62 USB3_TX3_P <<
```



Pair	Device
0	X
1	USB3.0, ext port1
2	X
3	USB3.0, ext port2
4	Bluetooth
5	X
6	X
7	X
8	X
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (Bluetooth)
12	CAMERA
13	X

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

OC[3:0]# for Device 29 (Ports 0-7)



```

1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

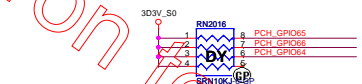
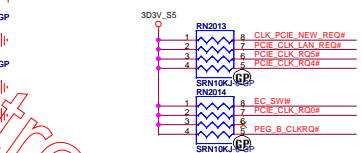
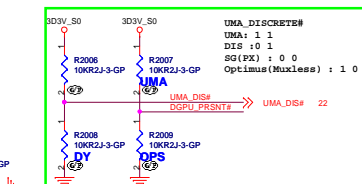
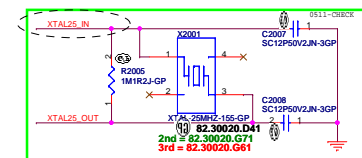
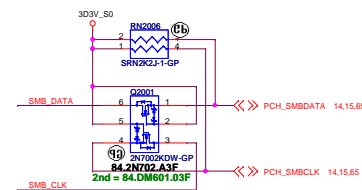
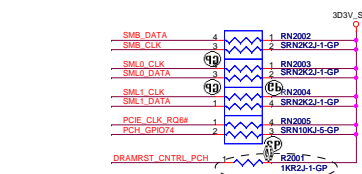
```

HIGH	Enabled (DEFAULT)
LOW	Disabled

PM_CLKRUN# R1909 1 BK2R2J-3-GP

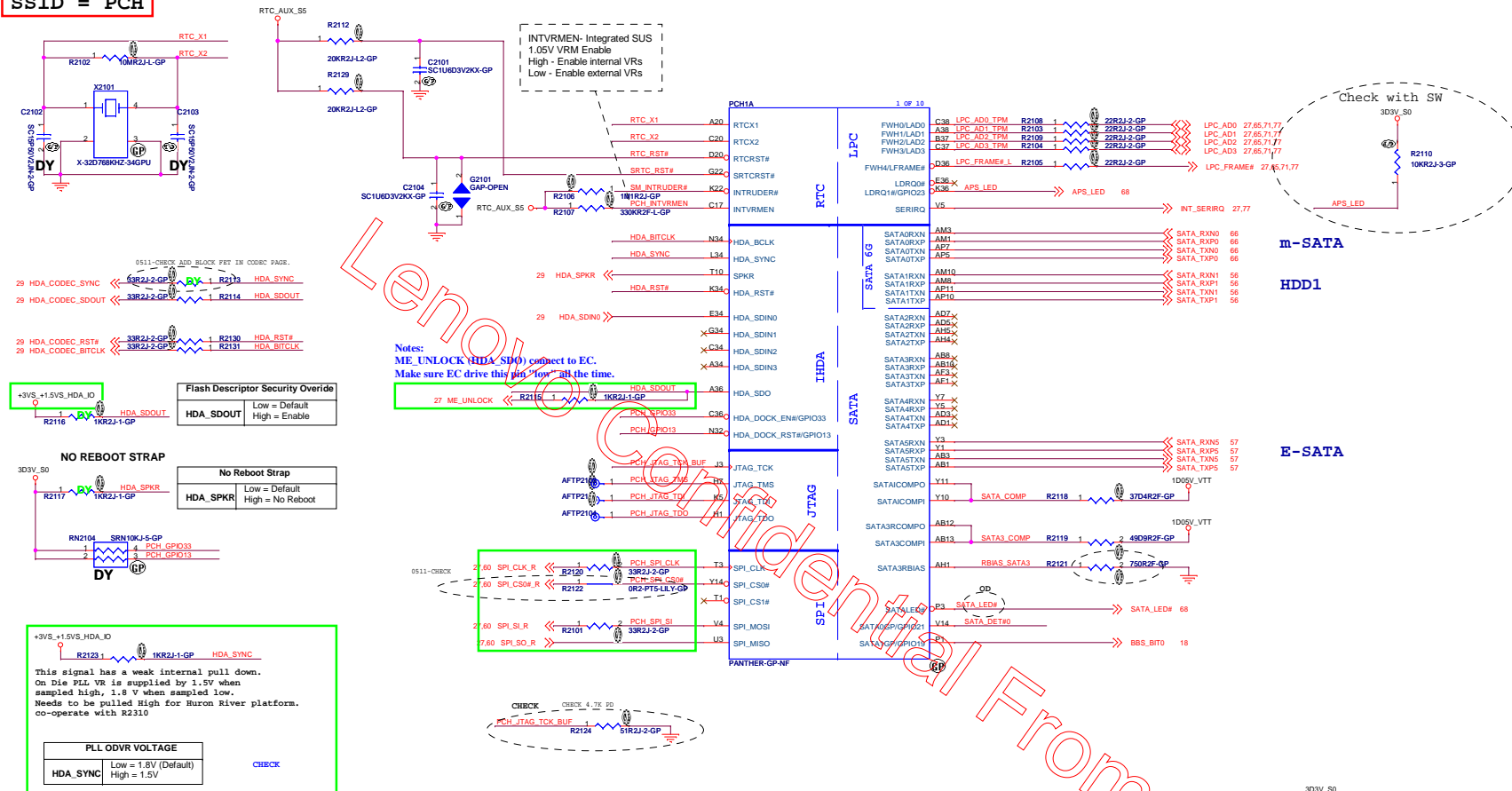
For platforms supporting DEEP S4/S5 state, a low on this signal indicates that PCN is in Deep Sleep state and that EC/platform logic does not need to keep the Suspend Rails ON.
If high means EC must keep SUS rails ON.
If DEEP S4/S5 is not supported, then this pin can be left unconnected.

If PCIE port 1 is disabled, it will cause all PCIE port disabled



Title			
PCH : PCIE/SMBUS/CLK			
Size A2	Document Number		Rev
	LGN-1		1
Date:	Wednesday, March 21, 2012	Sheet 20 of	103

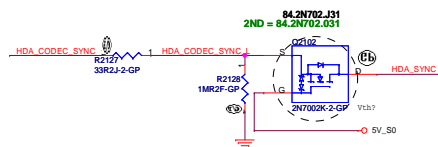
SSID = PCH

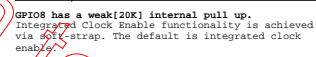


This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when
sampled high, 1.8 V from VccVRM when sampled low.

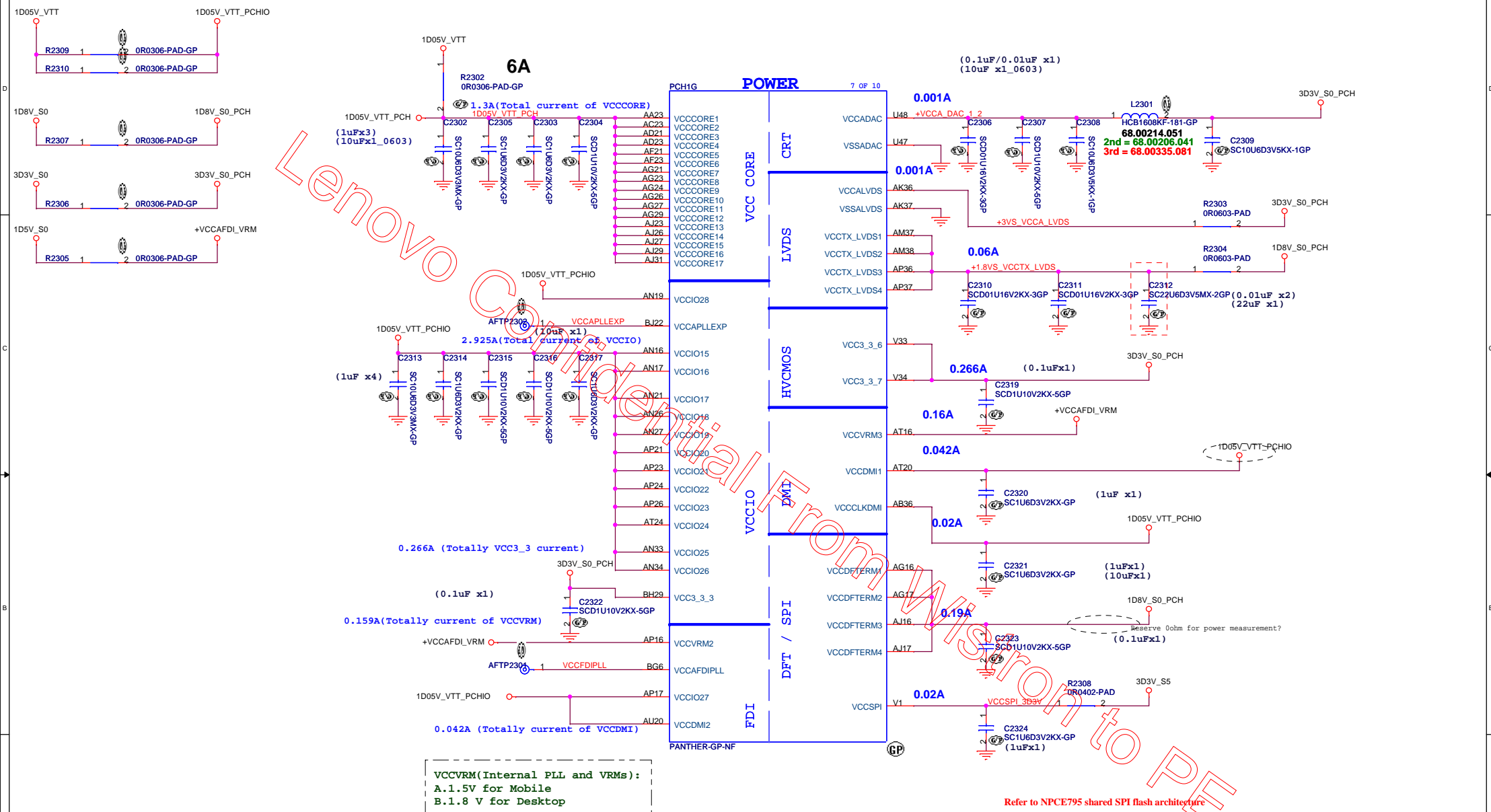
PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.



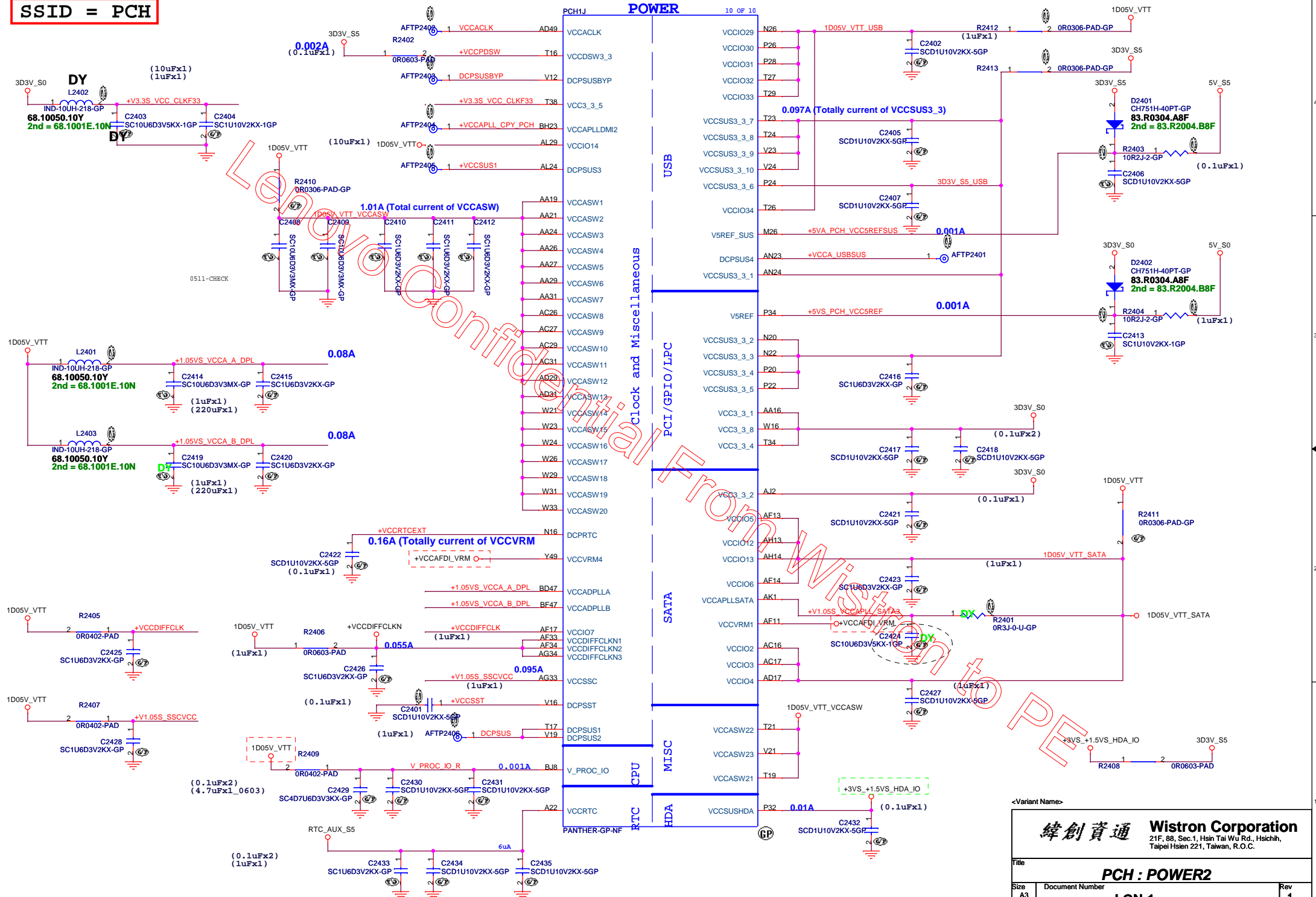


SSID = PCH

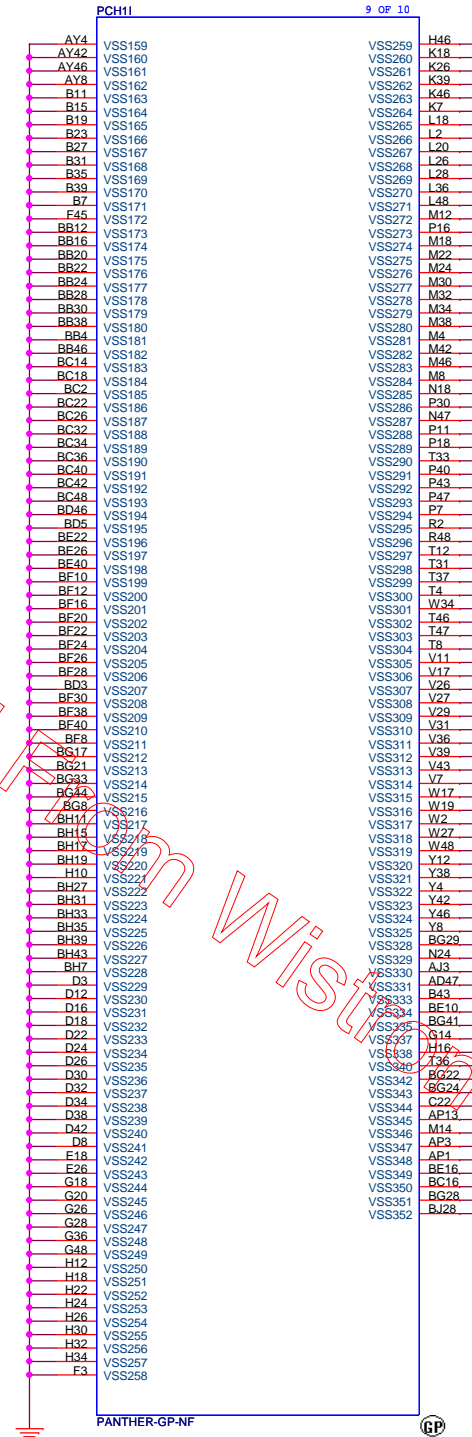
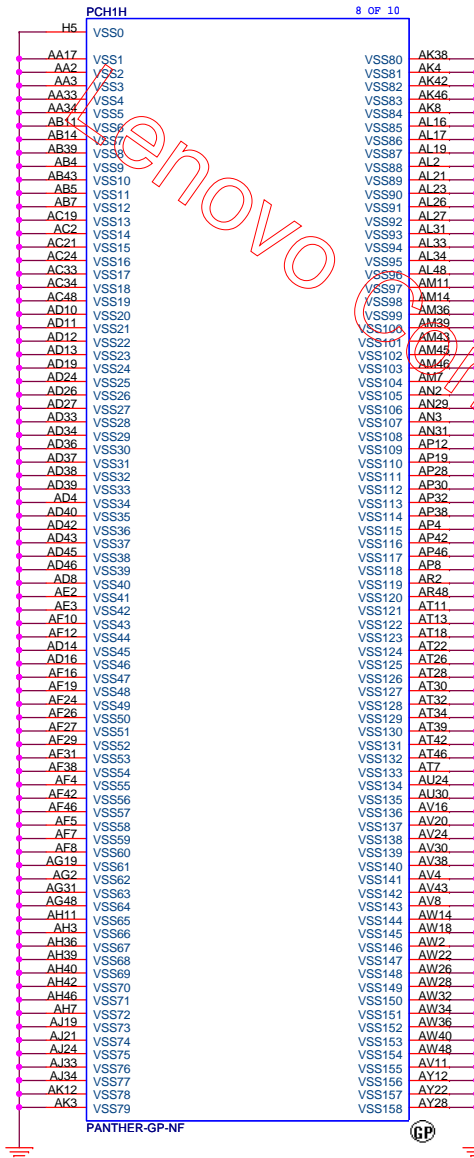


Refer to NPCE795 shared SPI flash architecture

SSID = PCH



SSID = PCH



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCH : VSS		
Size	Document Number	Rev
A3	LGN-1	1
Date:	Wednesday, February 15, 2012	Sheet 25 of 103

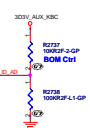
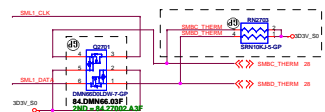
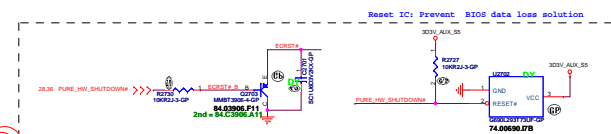
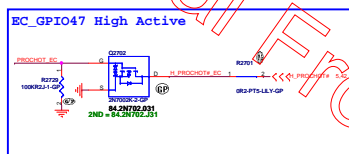
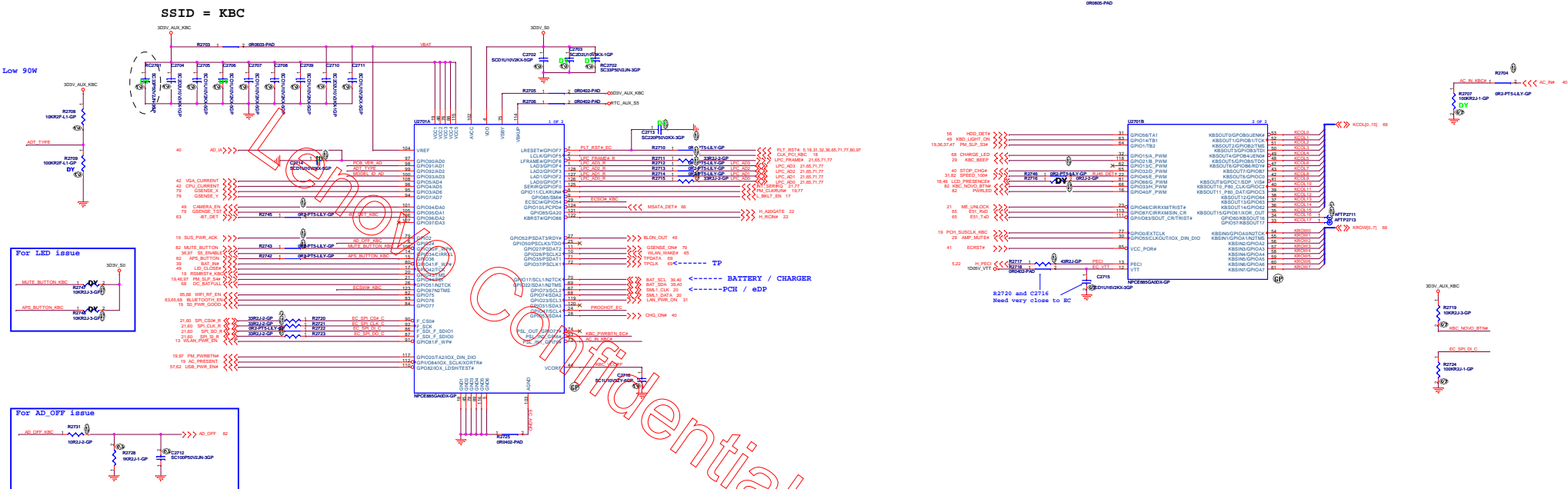
BLANK

Lenovo Confidential From Wistron to PE

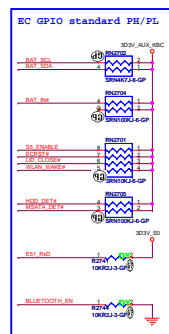
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 26 of	103

D65W_90W#
High: 65W / Low 90W



MODEL_ID_AD (Pin00)	Pull Down	Pull High	Voltage
UMA (LGN-1)	100.0K	10.0K	3.0V
UMA (LLP-1)	100.0K	20.0K	2.75V
OPTIMUS (LLG-1)	100.0K	33.0K	2.48V
UMA (LSS-1)	100.0K	47.0K	2.24V
OPTIMUS (LSS-1)	100.0K	64.9K	2.0V



PCB Version A2	Pull-Down Resistor (R_{PD})	Pull-Up Resistor (R_{PU})	Voltage
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V

71.00885.A0G
IC EMB CTRL NPCE885PA0DX LQFP 128P

Thermal sensor

T8

1

C

B

Q2802

SC390P50V2KX-GP

MMBT3904WT1G-GP1

CPU backside or inside the socket

2200p close to smsc2103 chip

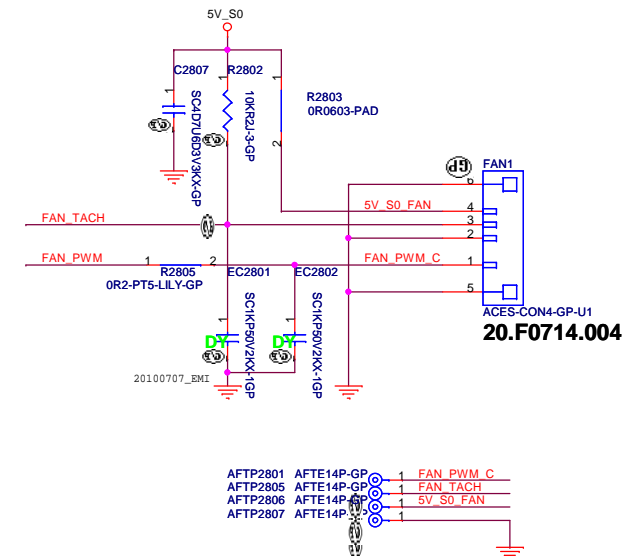
H.thermda

C2803

SC2200P50V2KX-2GP

H.thermdc

4 WIRE PWM Fan Control circuit



3D3V_S0

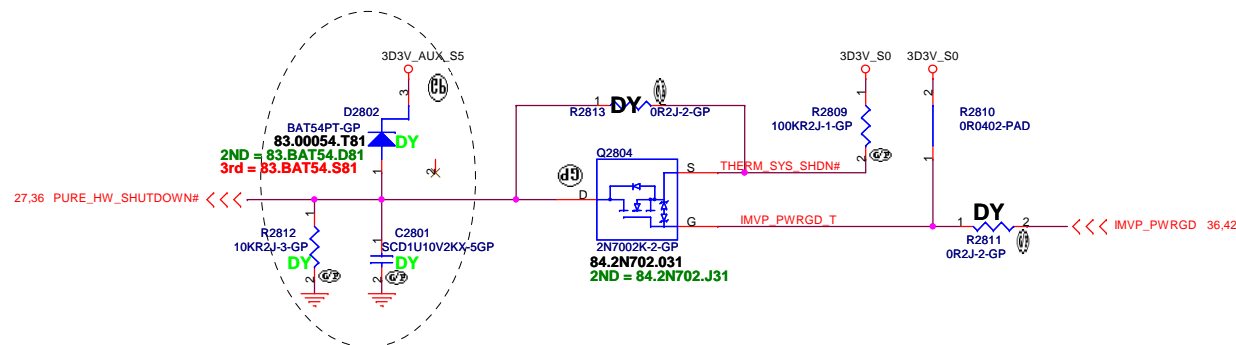
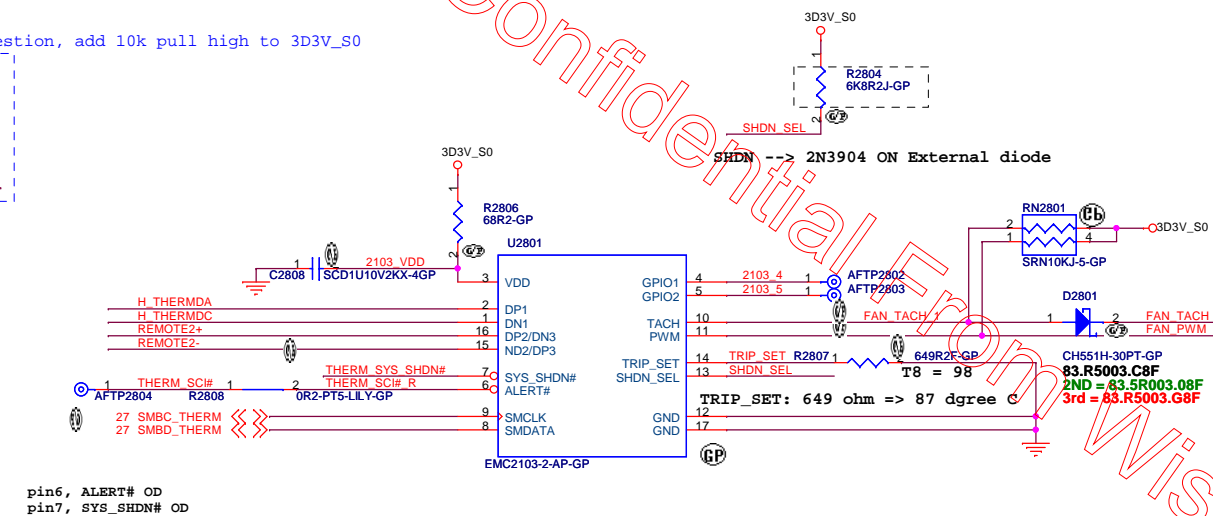
1

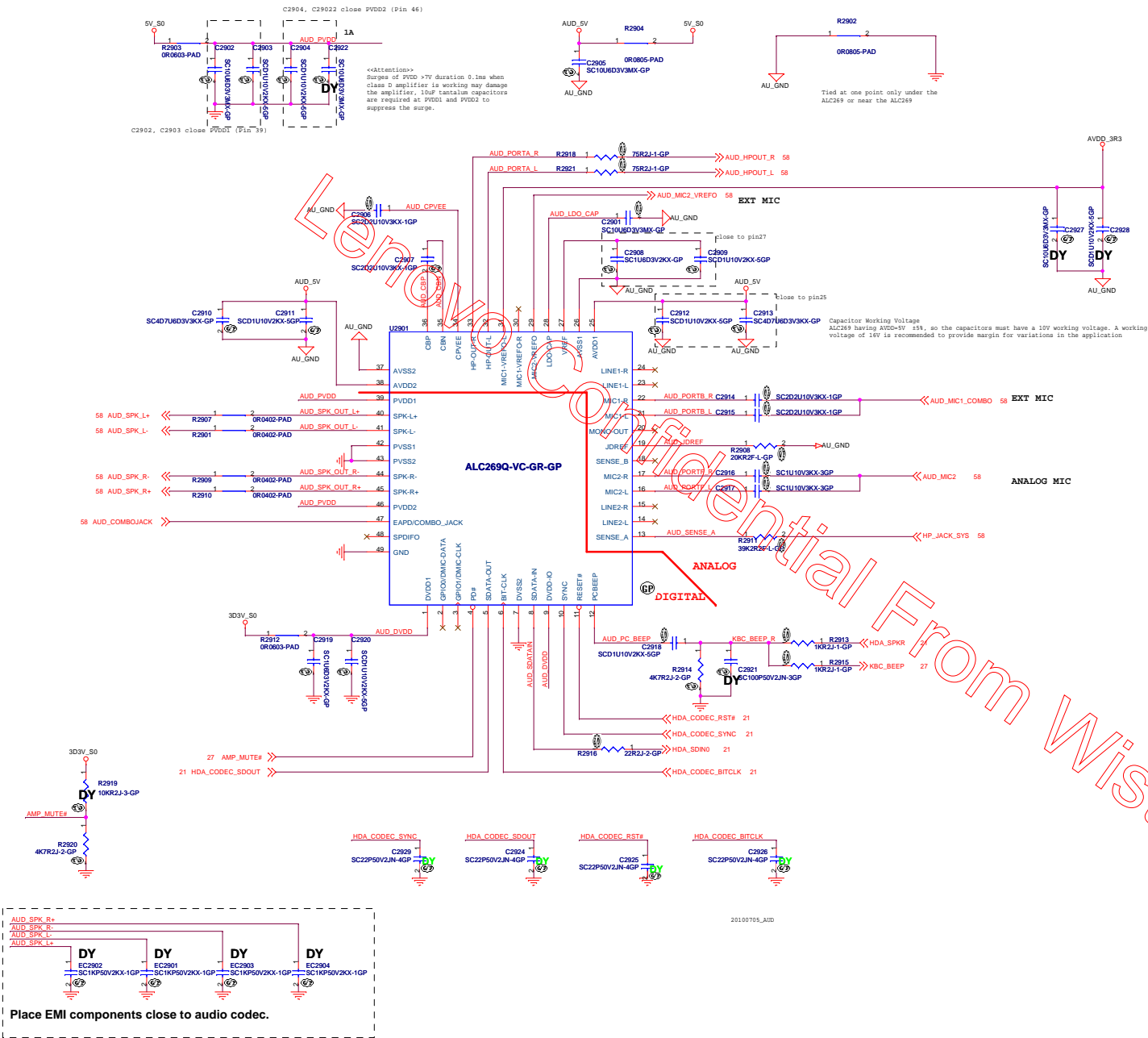
R2801
10KR2J-3-GP

2

Q2

THERM_SC#





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taipai Hsien 321, Taiwan, R.O.C.

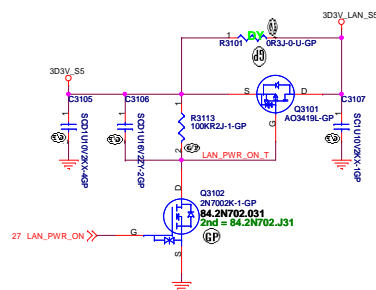
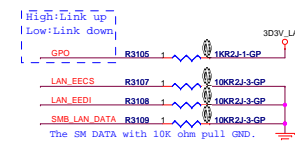
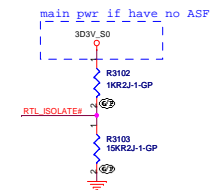
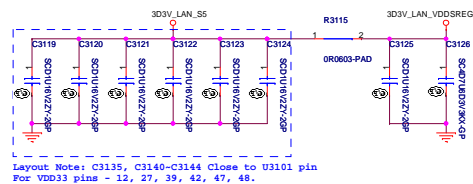
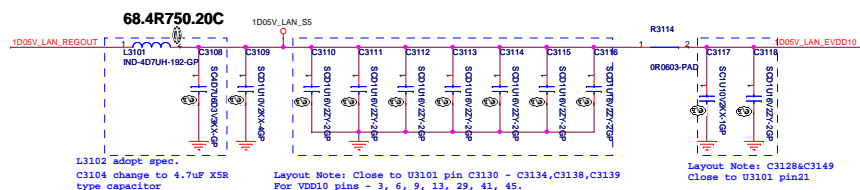
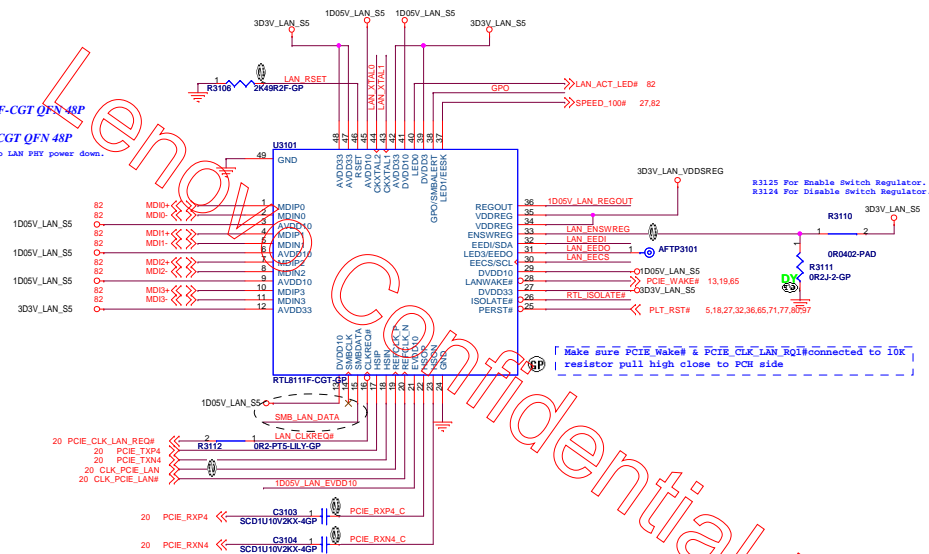
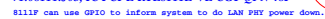
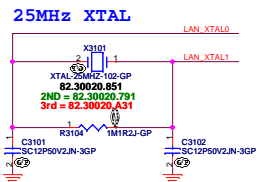
Title		
AUDIO CODEC		
Size	Document Number	Rev
Custom	LGN-1	1
Date	Wednesday, March 21, 2012	Sheet 29 of 103

Lenovo Confidential From Wistron to PE

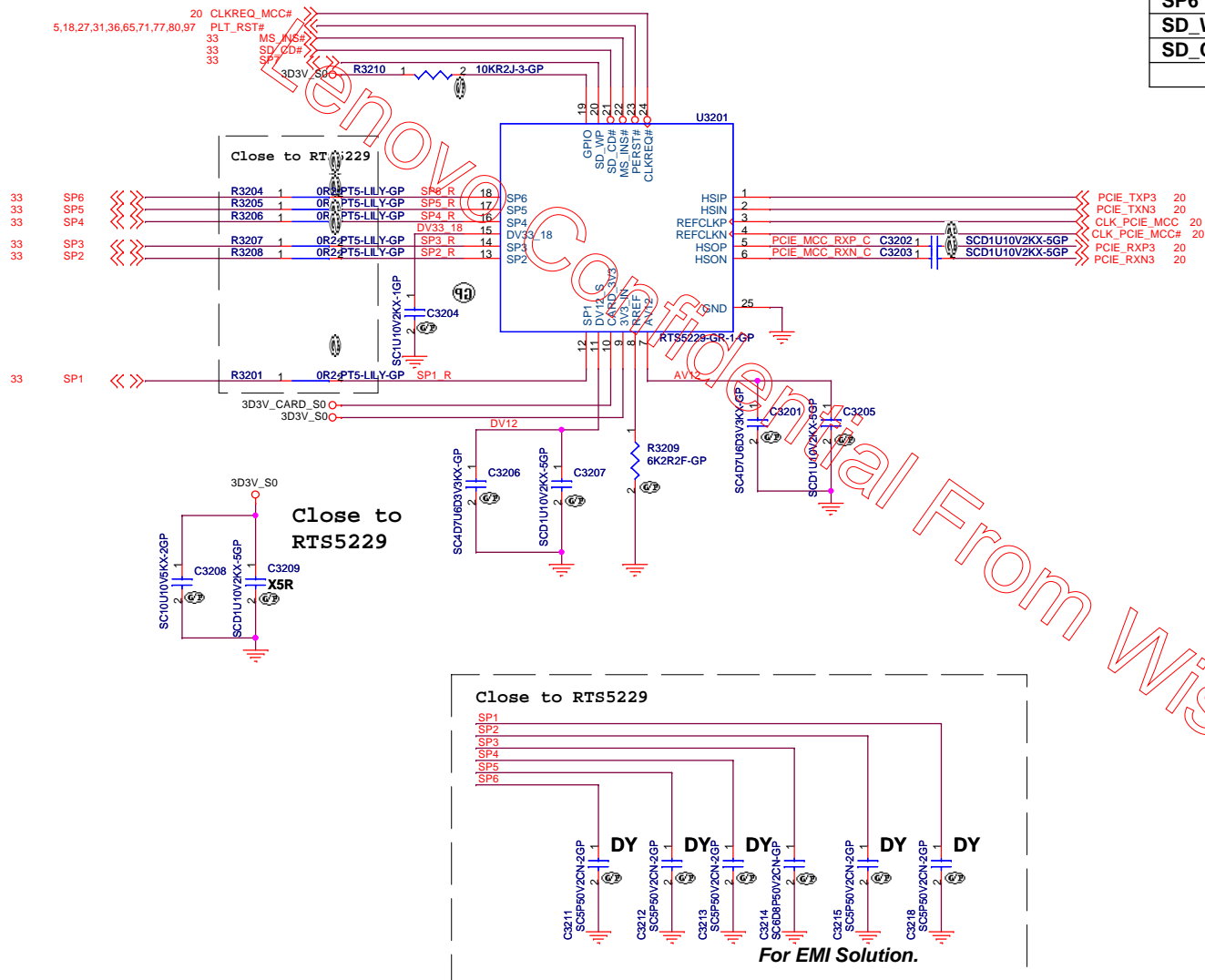
BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 30 of	103

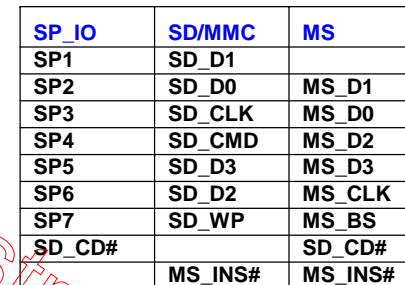


SP_IO	SD/MMC	MS
SP1	SD_D1	
SP2	SD_D0	MS_D1
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SD_WP	SD_WP	MS_BS
SD_CD#		SD_CD#
	MS_INS#	MS_INS#



<Variant Name>

AFTP3310 AFTE14P-GP



Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 34 of	103

Lenovo Confidential From Wistron to PE

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLANK

Size
A4

Document Number

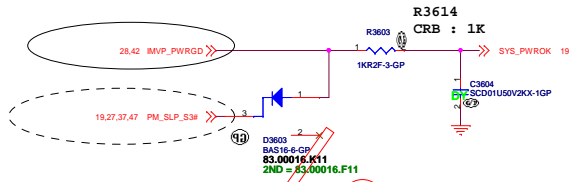
LGN-1

Rev
1

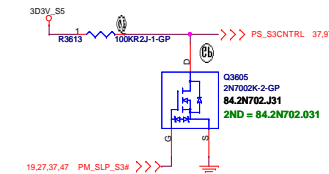
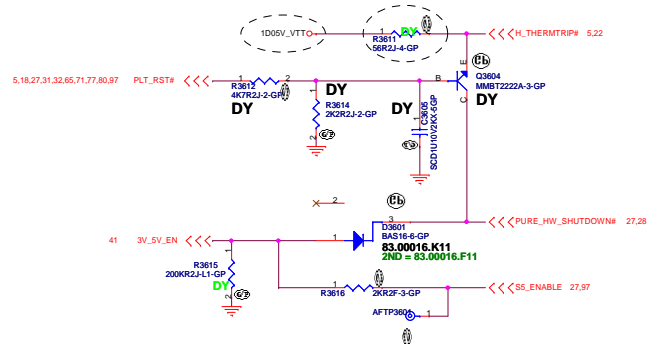
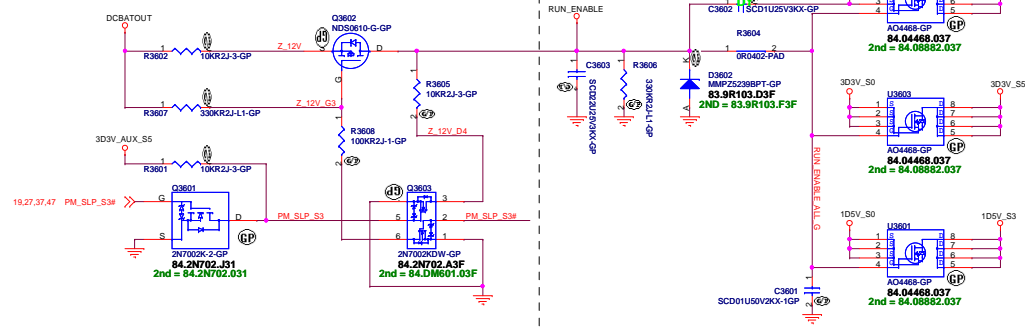
Date: Wednesday, February 15, 2012

Sheet 35 of 103

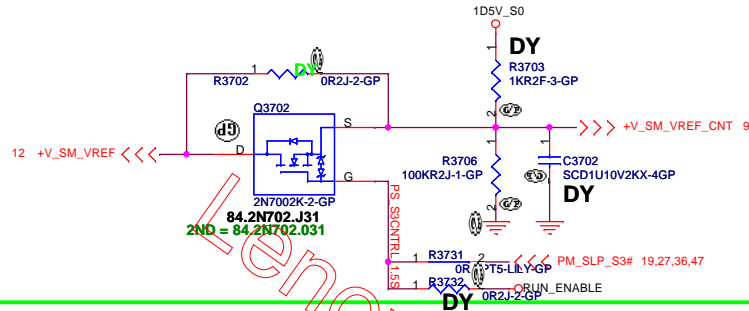
Power Sequence



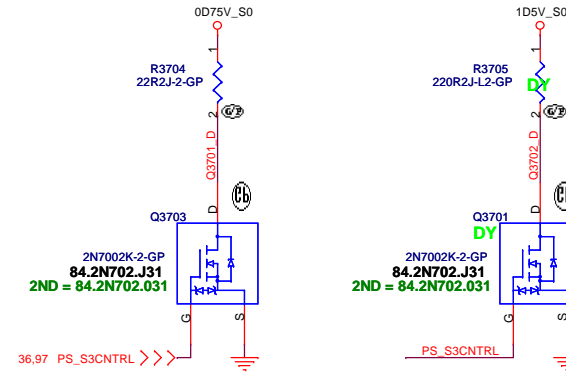
Run Power



Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

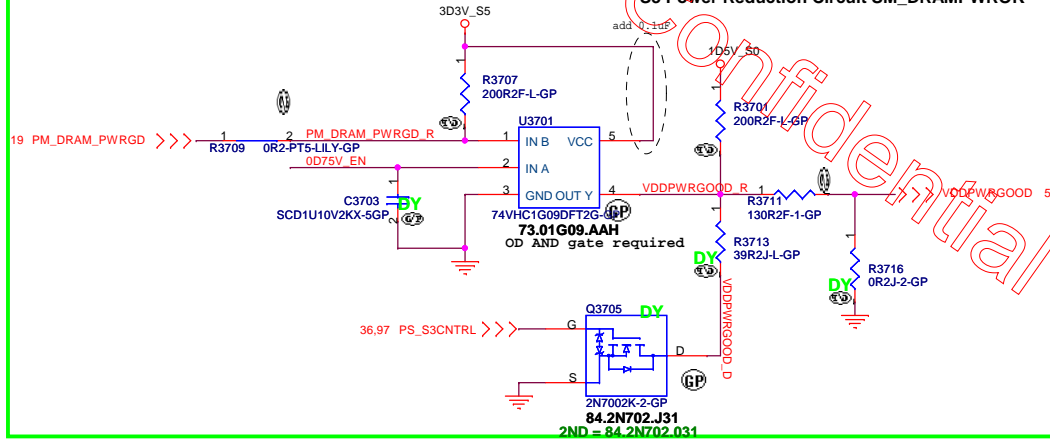


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

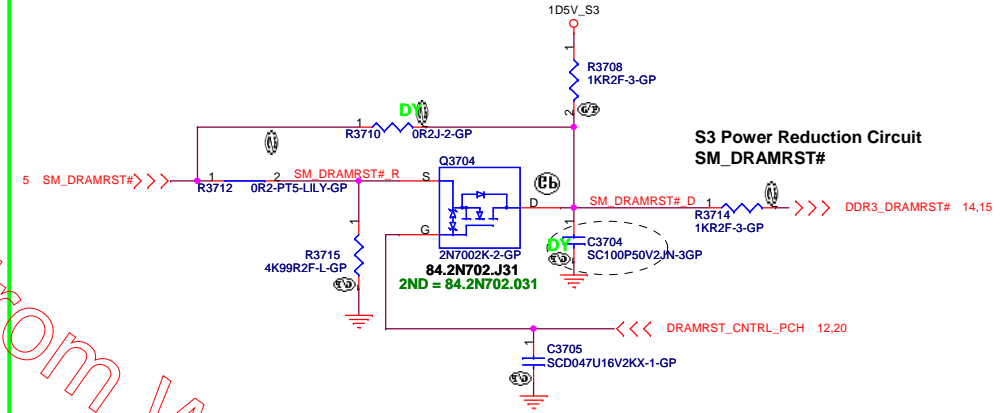


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

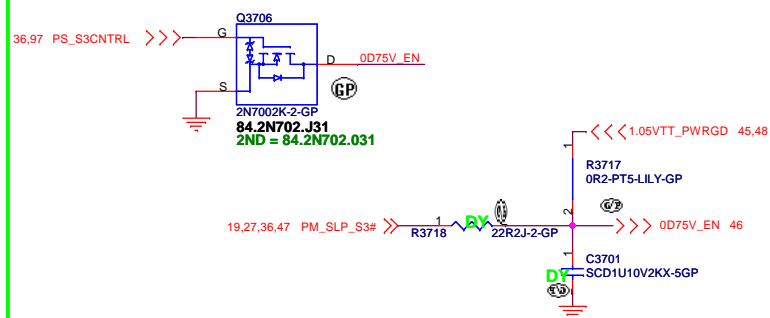
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



⑤ S3 Power Reduction



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

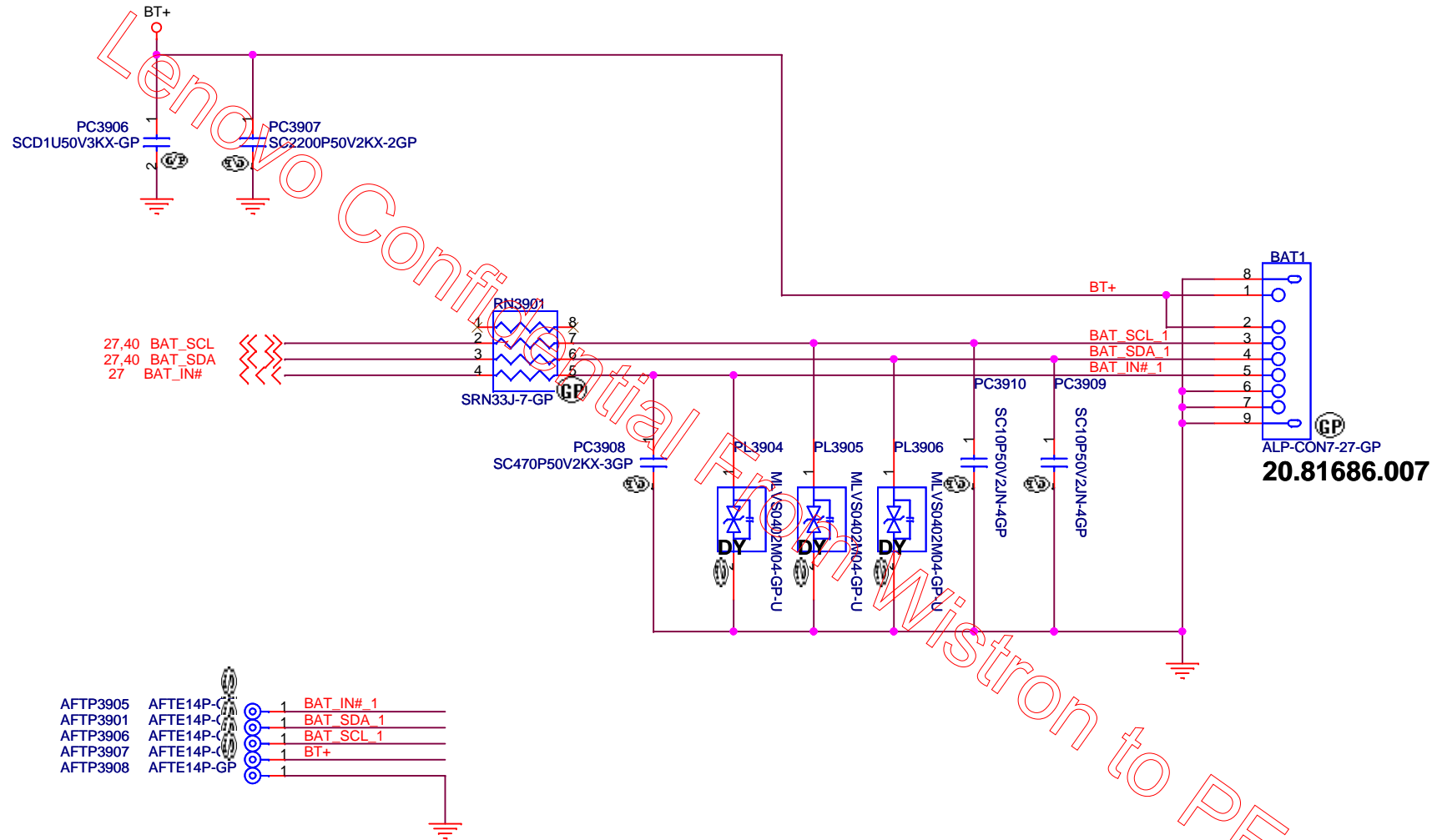
Title		
ADAPTER		
Size	Document Number	Rev
A3	LGN-1	1
Date: Wednesday, March 21, 2012		
Sheet 37 of 103		

Lenovo Confidential From Wistron to PE

JV10-CS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DCIN_JACK			
Size	Document Number		Rev
A3			1
Date:	Wednesday, February 15, 2012		Sheet 38 of 103

BATTERY CONNECTOR



JV10-CS

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BATT_CONN

Size

Document Number

LGN-1

Rev

1

Date: Wednesday, March 21, 2012

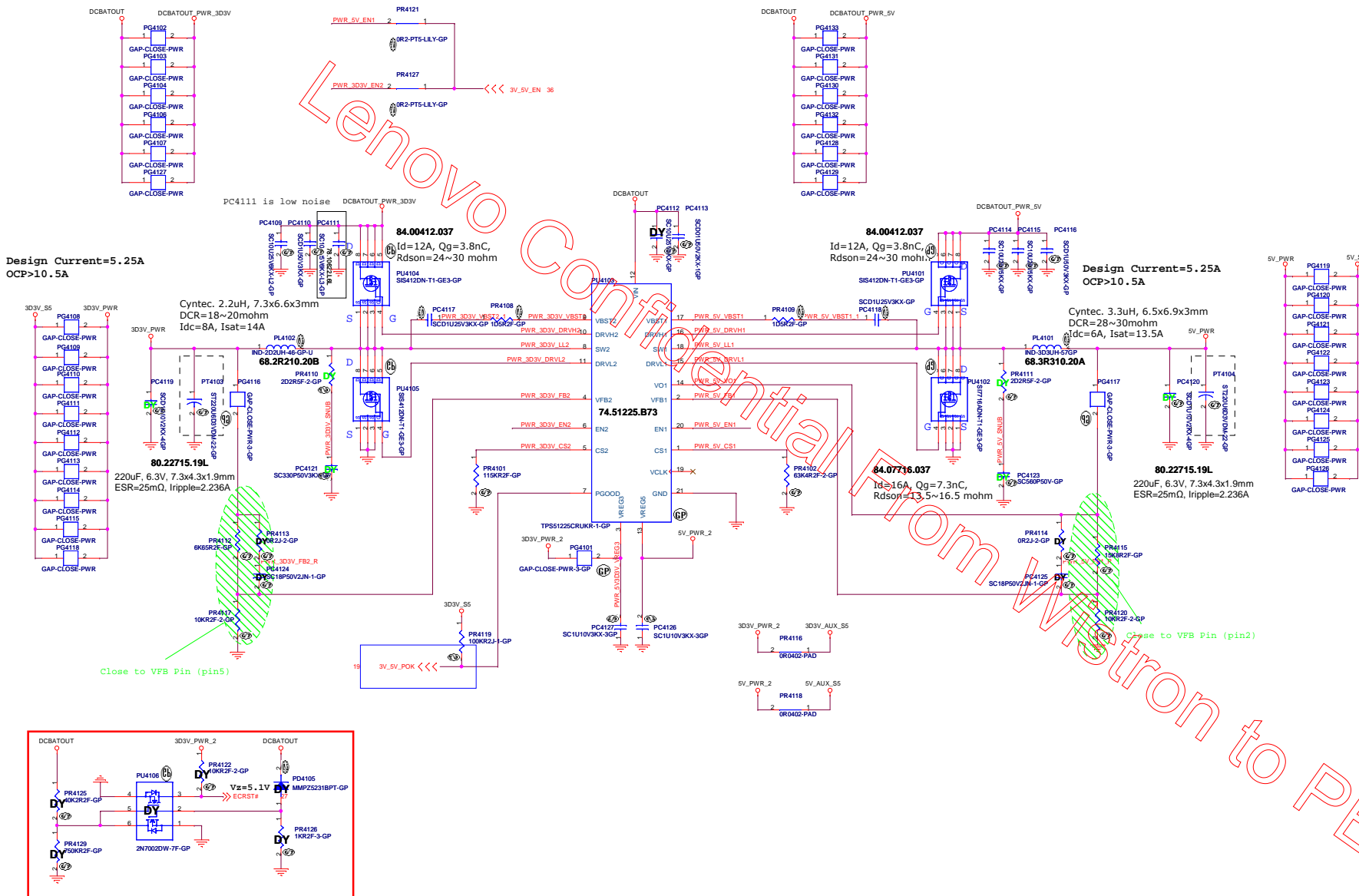
Sheet 39 of 103

A8(ANNIE/ASTRO)
PR4007,PR4008

STOP_CHG#
connects to KBC

Charger Current=1.4~3.6A

SSID = PWR.Plane.Regulator_5v3p3v



JV10-CS

42 PWR_CPU_CORE_CDHI >>>

42 PWR_CPU_CORE_CSW1 >>>

PWR_CPU_CORE_CBST1.1

PR4302

0R0603-PAD

42 PWR_CPU_CORE_CBST1 >>>

42 PWR_CPU_CORE_CDL1 >>>

20111209 Power

Power Team Remind:
This is to remind you made use of dual-N mosfet
about On-Semi or AOS solution caused
burn situation have to attention some recommends.

Your symbol part number has changed from
original p/n to ZZ.00215.037 to avoid burn
scenario occur.

Q1: Id=10.5A, Qg=8.9~17.3nC,
Rdson=10~13.6 mohm
Q2: Id=14A, Qg=10~21.2nC,
Rdson=6~8 mohm

42 PWR_CPU_CORE_CDHI >>>

42 PWR_CPU_CORE_CSW2 >>>

PWR_CPU_CORE_CBST2.1

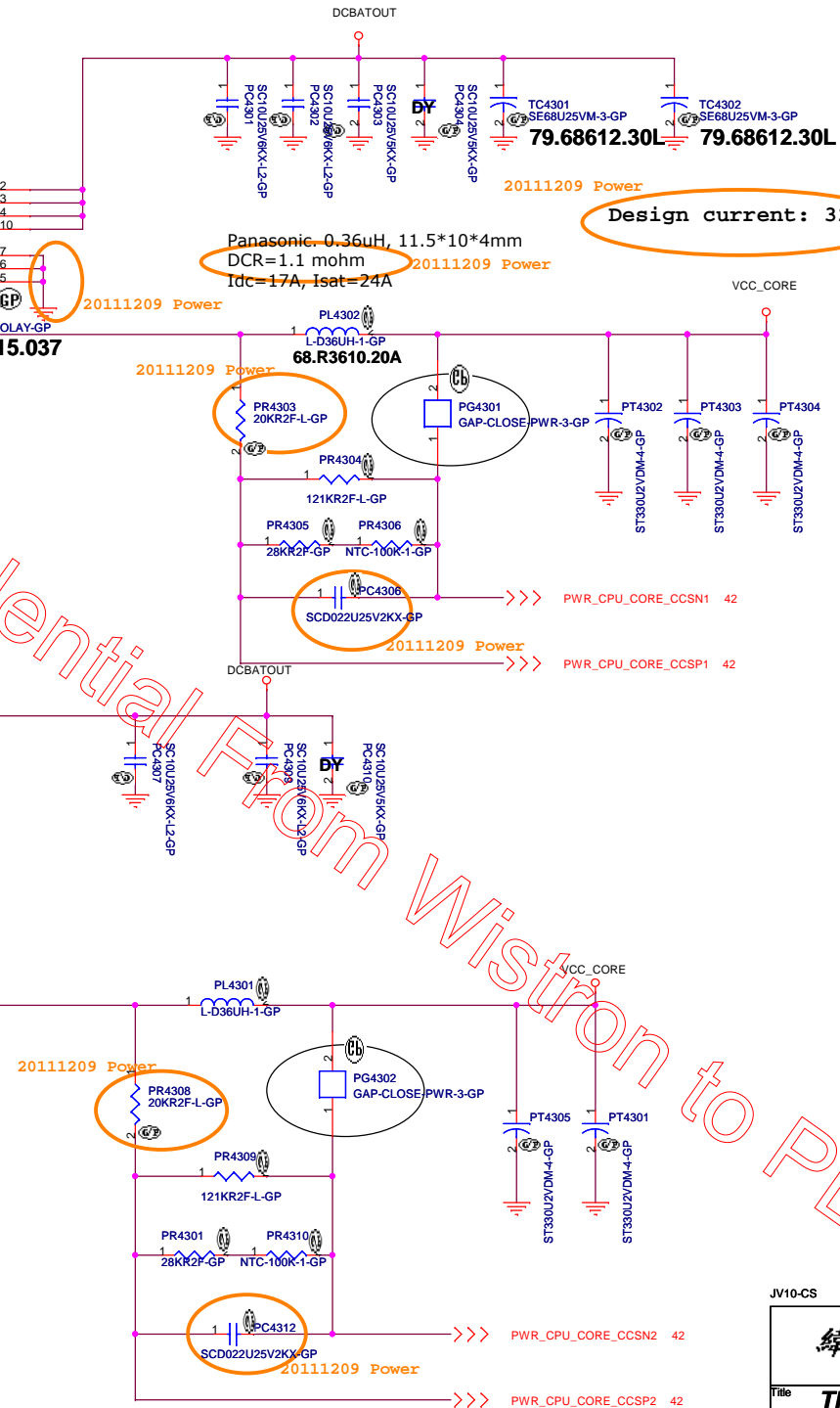
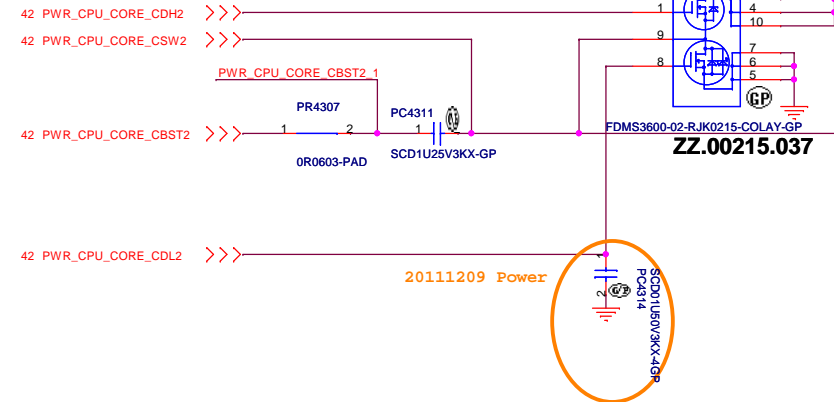
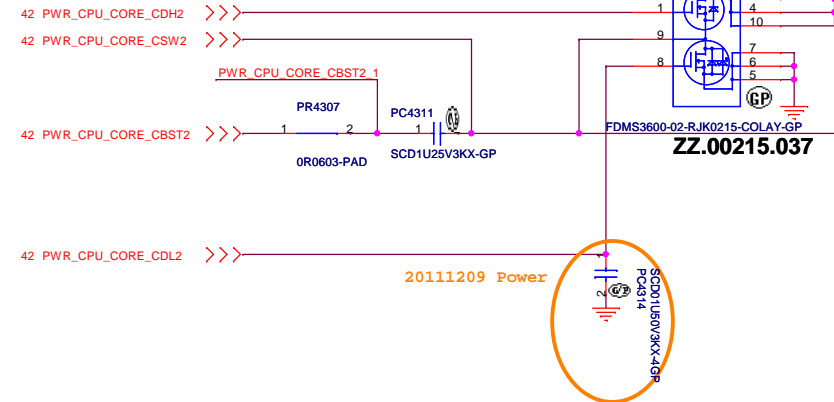
PR4307

0R0603-PAD

42 PWR_CPU_CORE_CBST2 >>>

42 PWR_CPU_CORE_CDL2 >>>

20111209 Power



JV10-CS

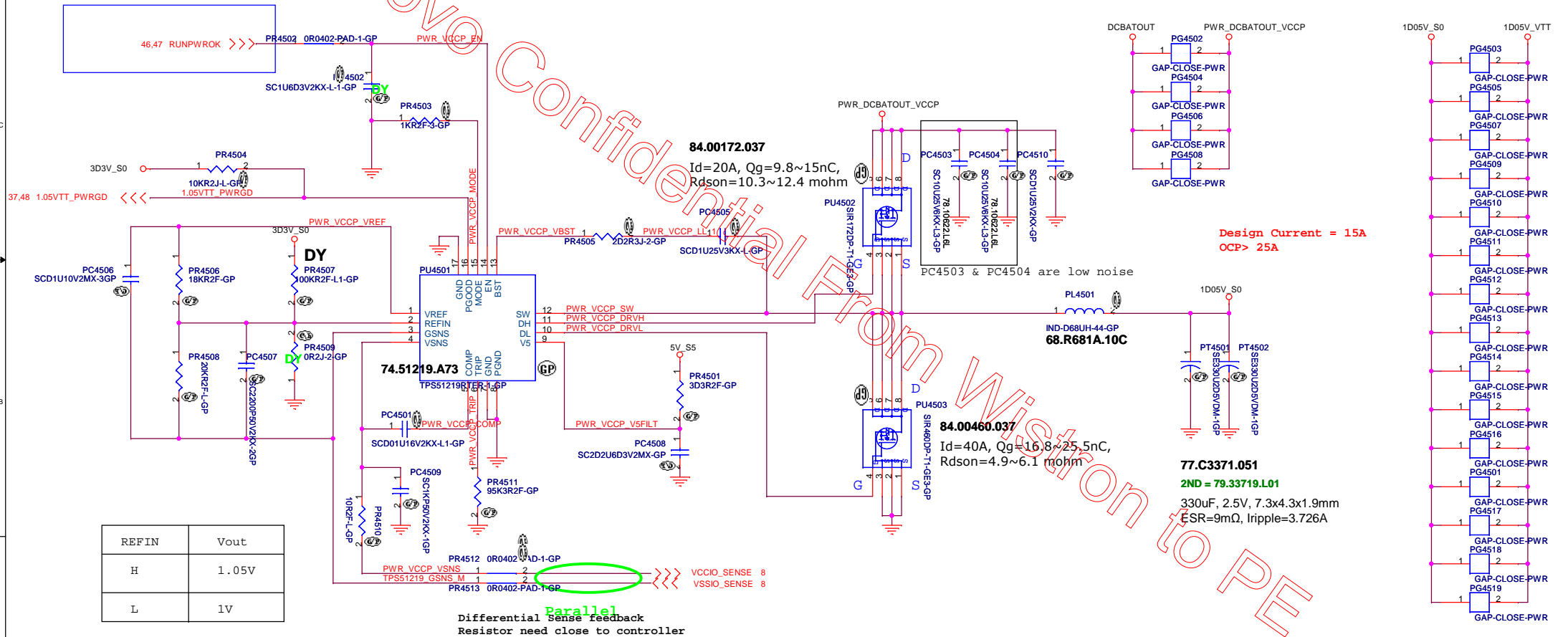
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title TPS51640_CPU_CORE(2/3)

Size Document Number LGN-1 Rev 1

Date: Wednesday, March 21, 2012 Sheet 43 of 103

TPS51219 for 1D05V



JV10-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			TPS51219_1D05V
Size	Document Number	LGN-1	
Date:	Wednesday, March 21, 2012	Sheet	45 of 103
Rev	1		

JV10-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **RT8207M_1D5V_0D75V**

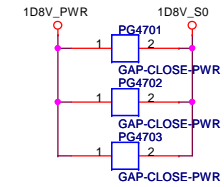
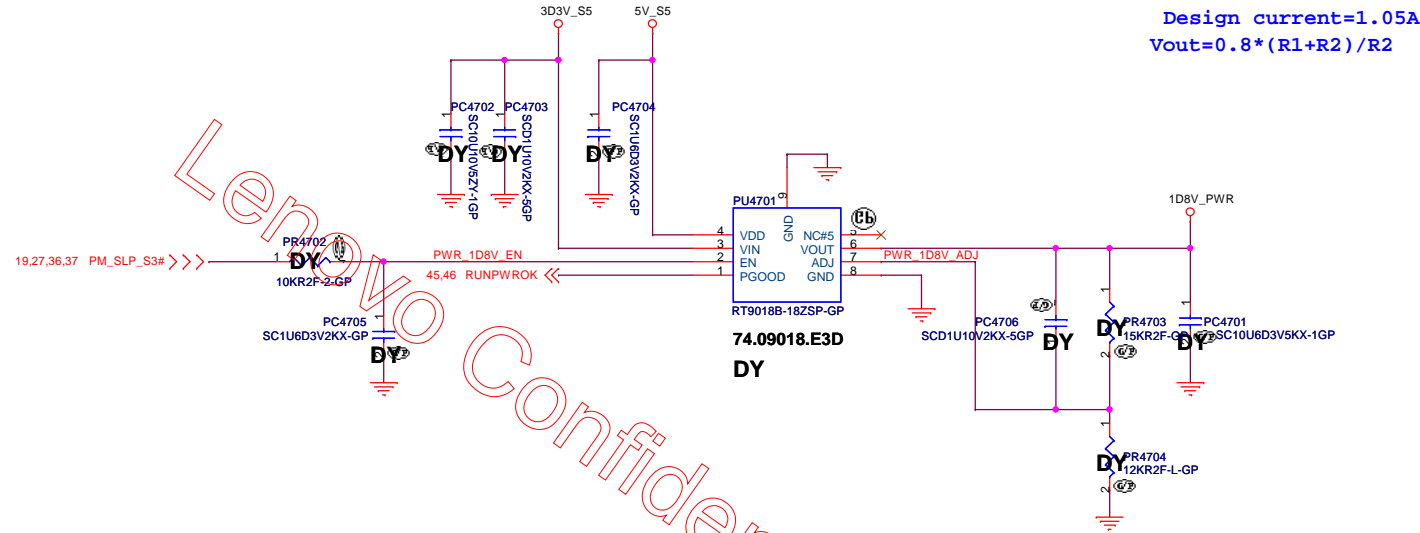
Size	Document Number	LGN-1
------	-----------------	--------------

Rev
1

Date: Wednesday, March 21, 2012 Sheet 46 of 103

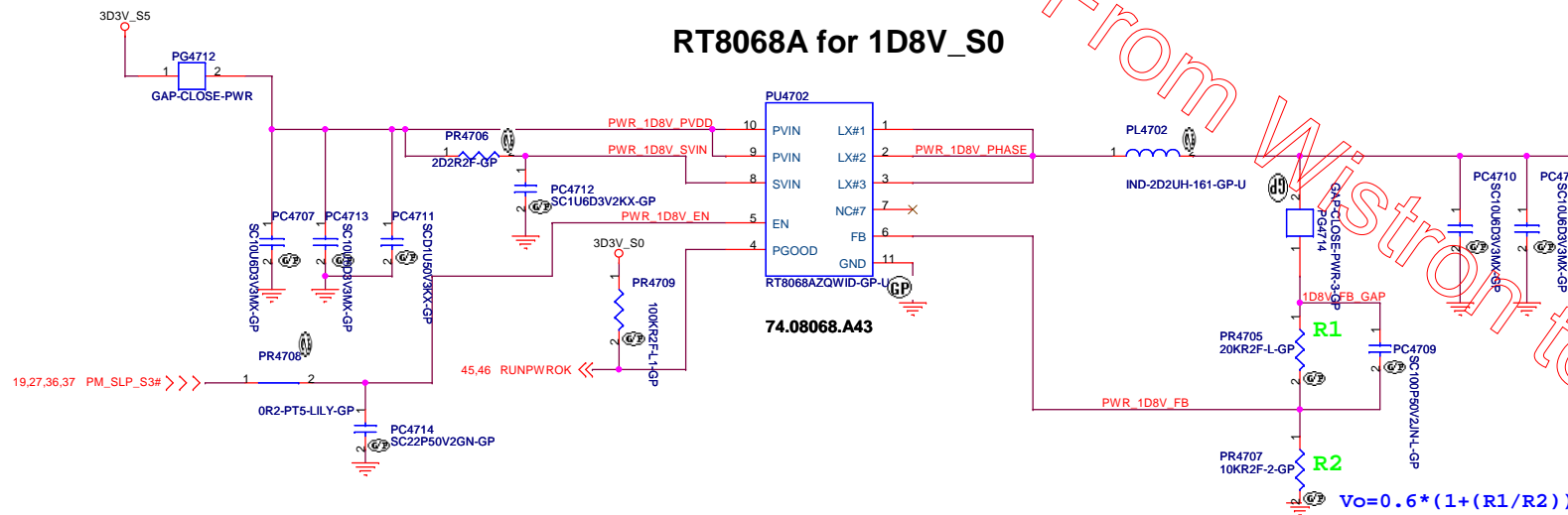
SSID = PWR.Plane.Regulator_1p8v

RT9018B-18ZSP for 1D8V_S0



RT8068A for 1D8V_S0

Design Current=1.1A

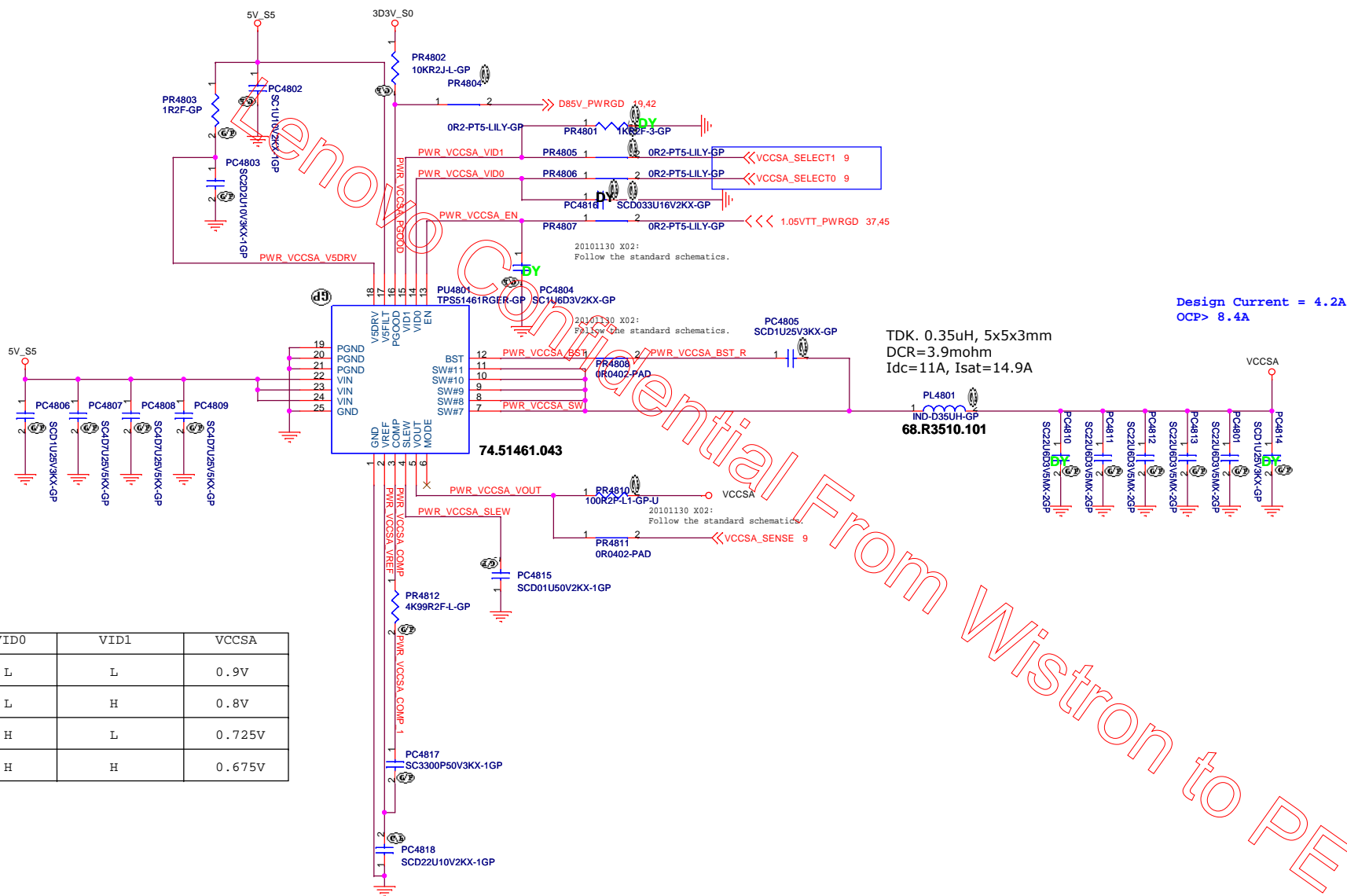


JV10-CS

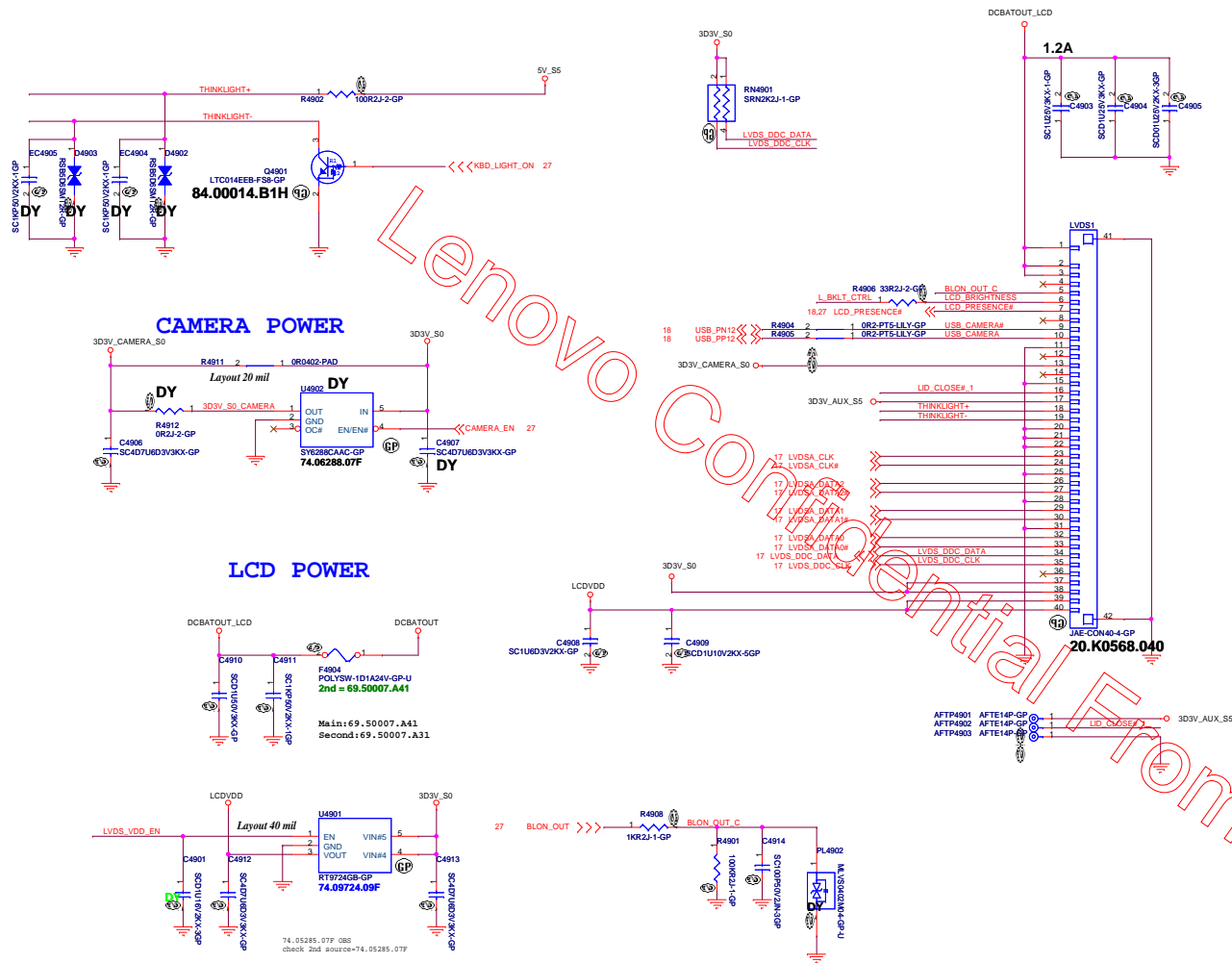
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			PWM_1D8V_RT9018B-18ZSP
Size	Document Number	Rev	1
LGN-1			
Date:	Wednesday, March 21, 2012	Sheet	47 of 103

TPS51461 for VCCSA

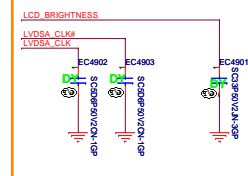


VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

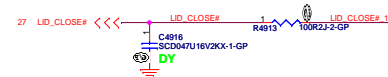


For EMI request
Close to LVDS connector

Panel BL brightness/Power En/BL En



HALL SENSE



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih

Title

LCD Connector

Size	Document Number
Custom	1 0 0 0 0

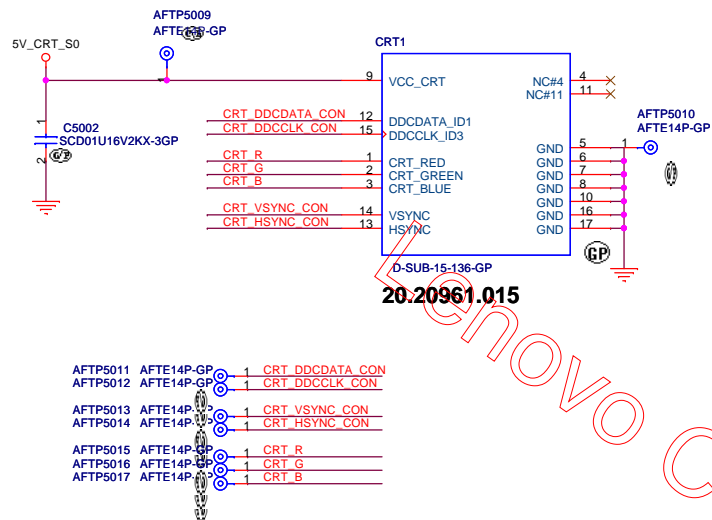
Number 1000000

Rev	
-----	--

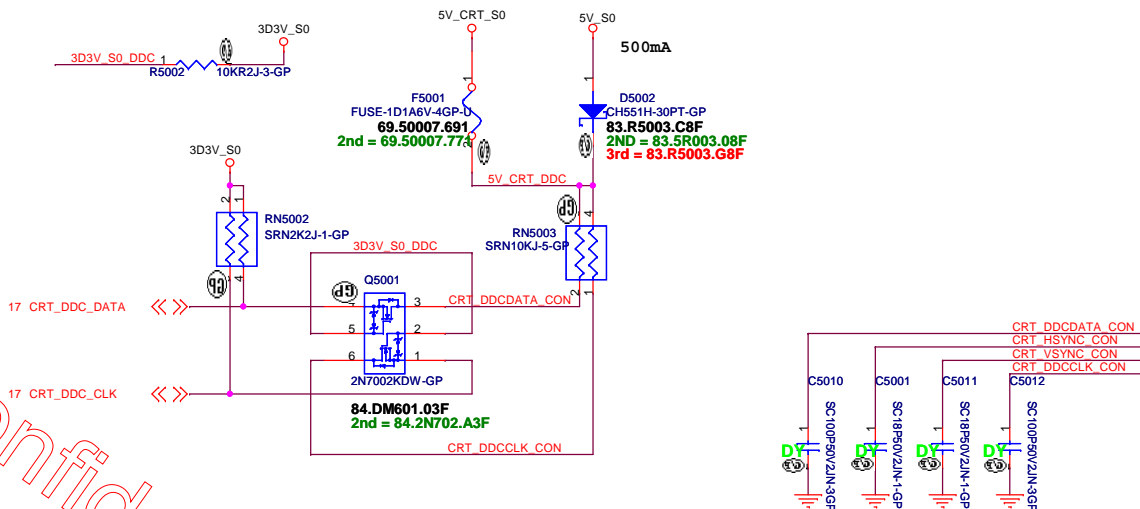
Custom	LGN-1
--------	--------------

	1
--	----------

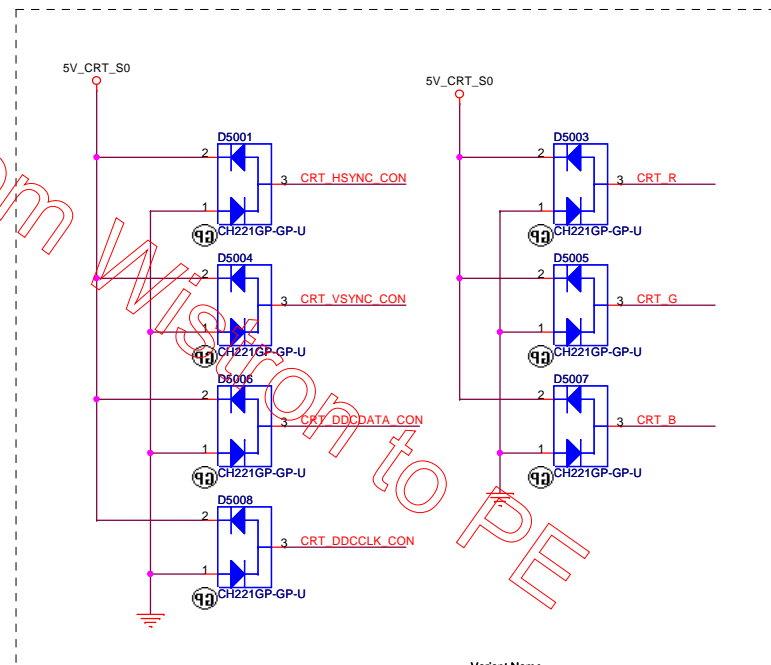
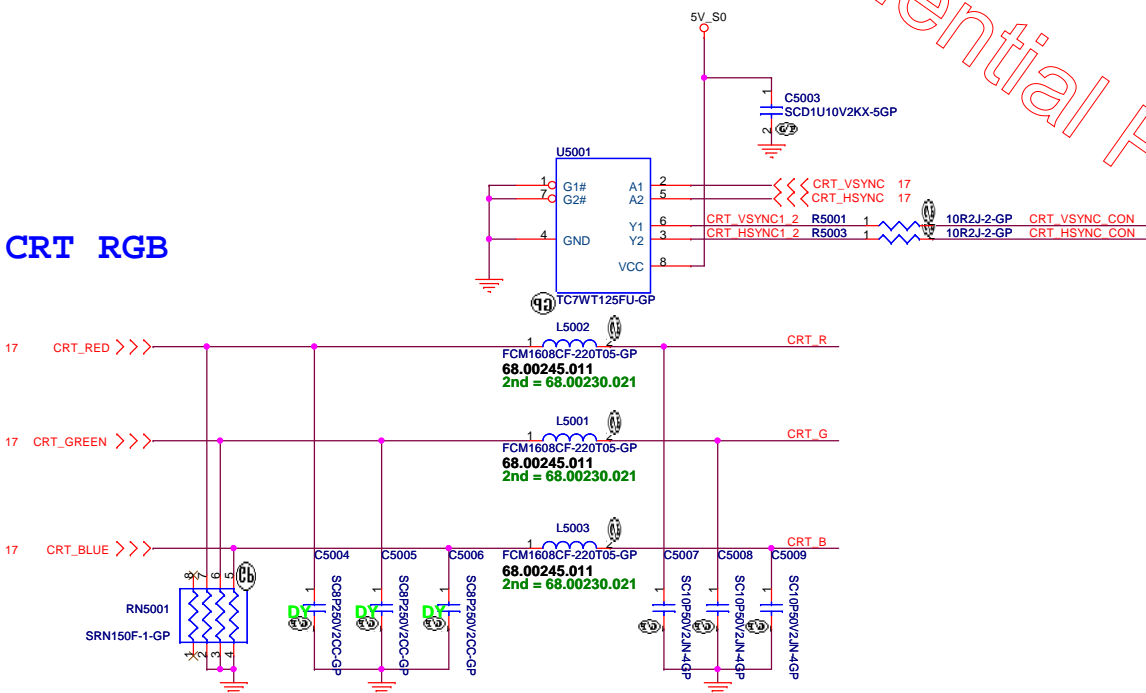
CRT connector



CRT DDCDATA & DDCCLK level shift



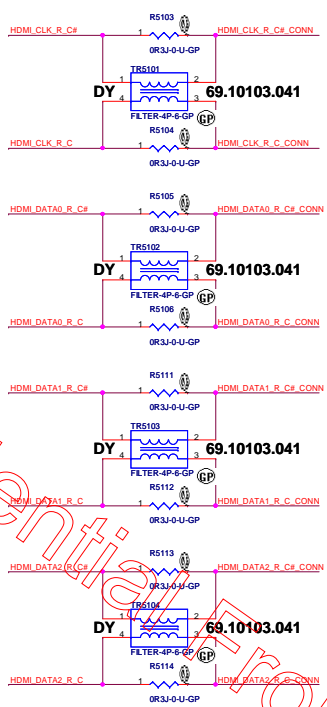
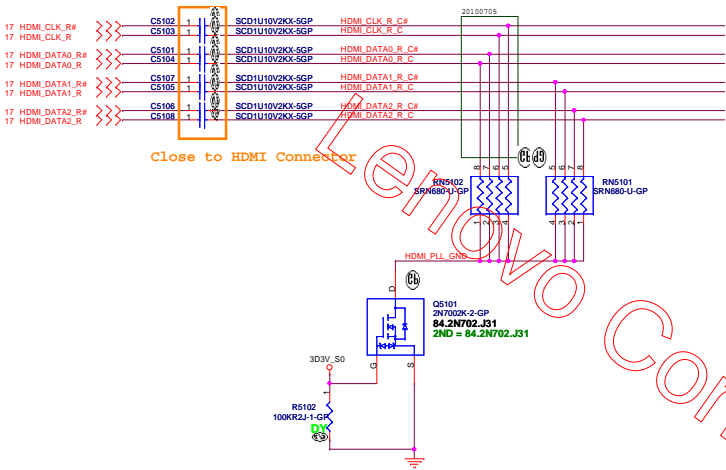
CRT Hsync & Vsync level shift



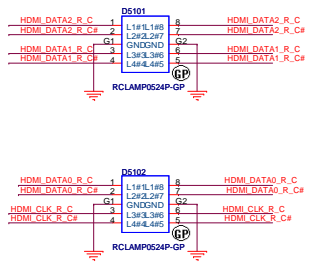
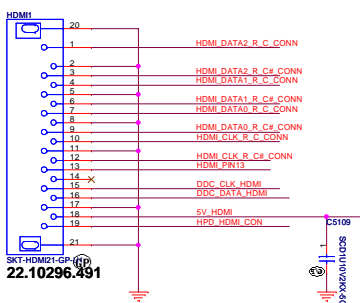
SSID = VIDEO

HDMI Passive Level Shifter

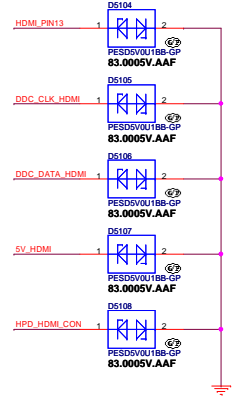
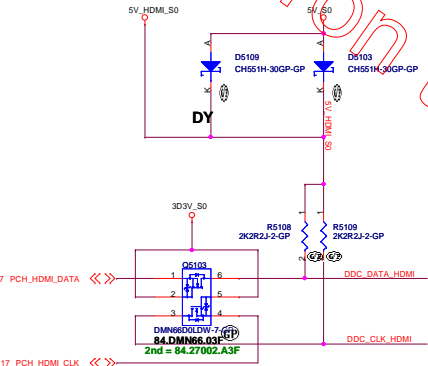
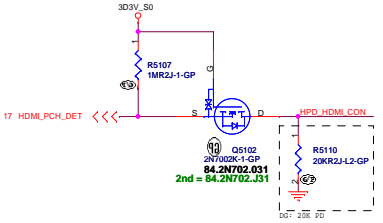
Close to HDMI Connector



HDMI CONNECTOR



HDMI DDC Passive Level Shifter



Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
eDP			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 52 of	103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
S-VIDEO			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 53 of	103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

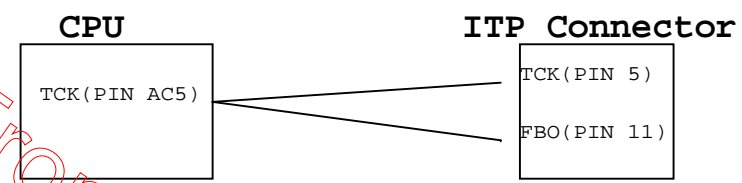
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 54 of	103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

Lenovo Confidential From Wistron to PE



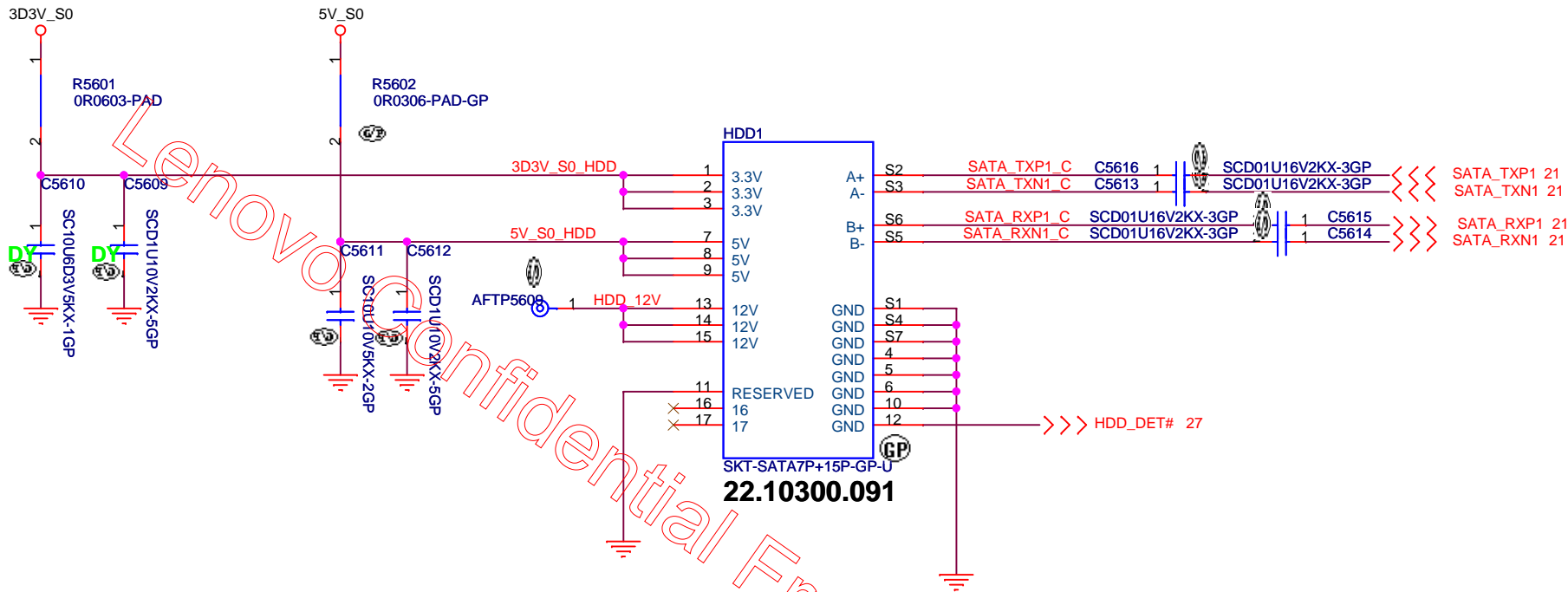
<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				
ITP				
Size A4	Document Number			Rev
	LGN-1			1
Date:	Wednesday, February 15, 2012		Sheet 55 of	103

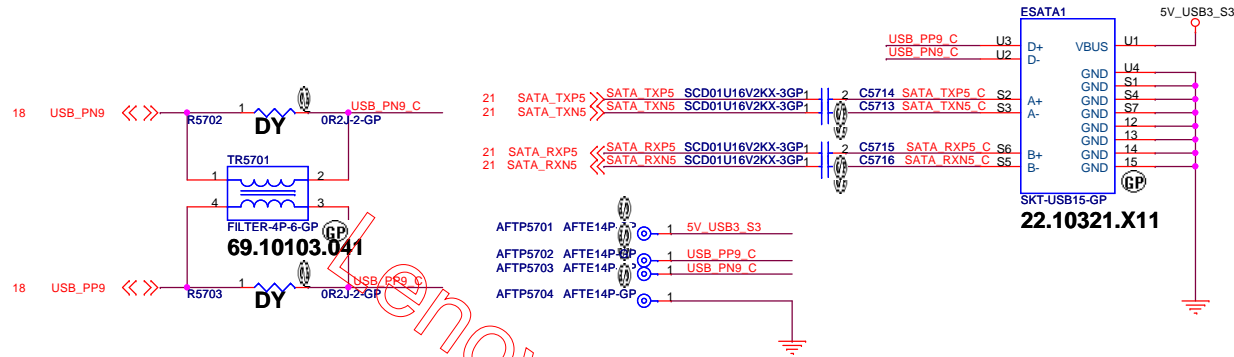
SATA HDD Connector



22.10300.091

<Variant Name>

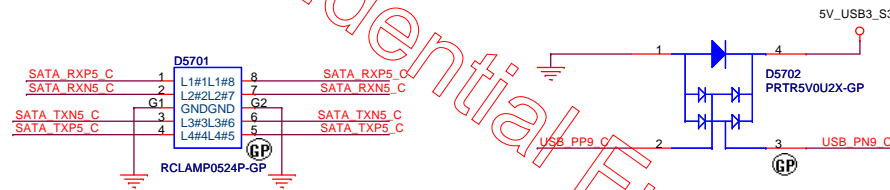
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD/ODD			
Size A4	Document Number LGN-1		Rev 1
Date:	Wednesday, March 21, 2012	Sheet 56 of	103



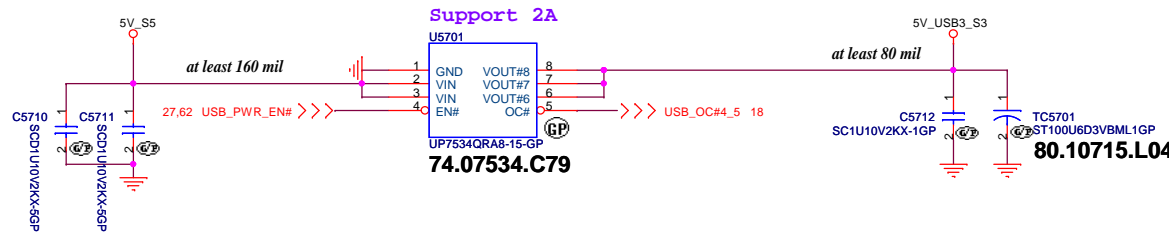
ESATA	
NAME	TYPE
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
USB	
NAME	TYPE
U1	VBUS
U2	D-
U3	D+
U4	GND

ESATA

ESD Protection



POWER



<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ESATA or USB20			
Size A3	Document Number LGN-1		Rev 1
Date: Wednesday, March 21, 2012			
Sheet		57	of 103

Int. Mono Analog MIC for B series

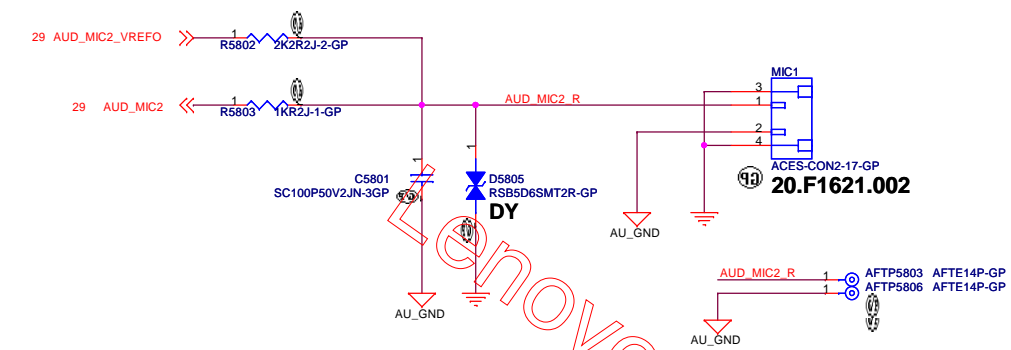
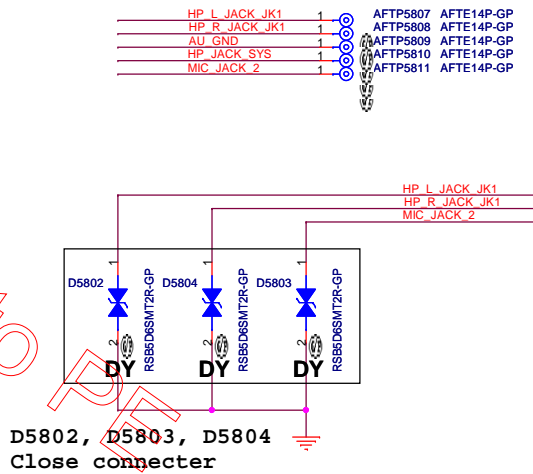
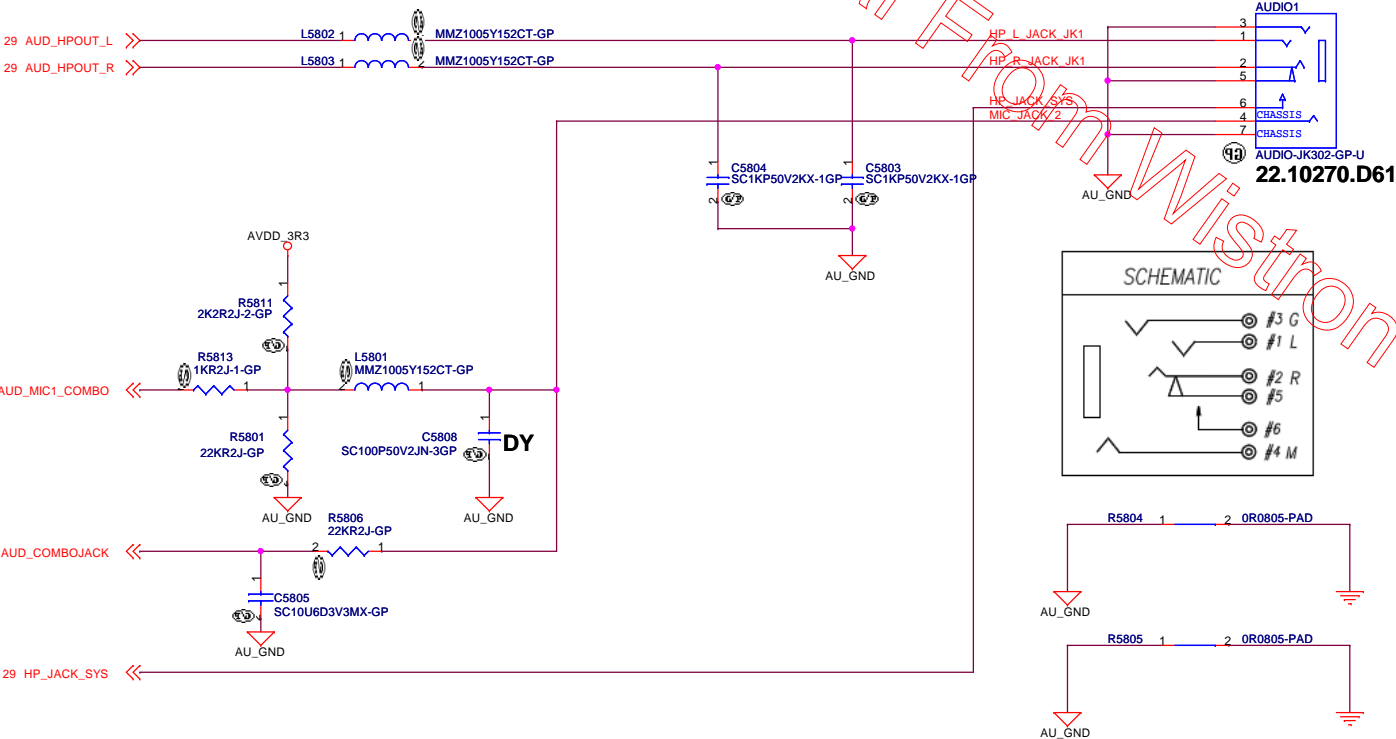
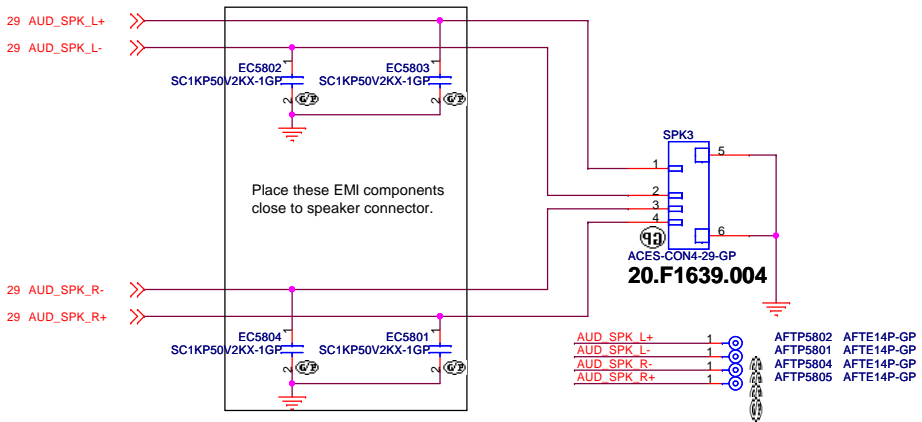


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

INTERNAL STEREO SPEAKERS



Lenovo Confidential From Wistron to PE

<Variant Name>			
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
RJ45 / Transformer			
Size	Document Number		Rev
A3	LGN-1		1
Date:	Wednesday, February 15, 2012	Sheet	59 of 103

SPI FLASH ROM (8M byte) for PCH



AFTP6001 AFTE14P-GP 1 +RTC_VCC
AFTP6002 AFTE14P-GP 1

緯創資通

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Flash/RTC

LGN-1

Rev
1

Sheet 60 of 103

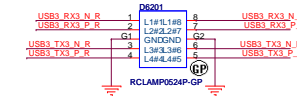
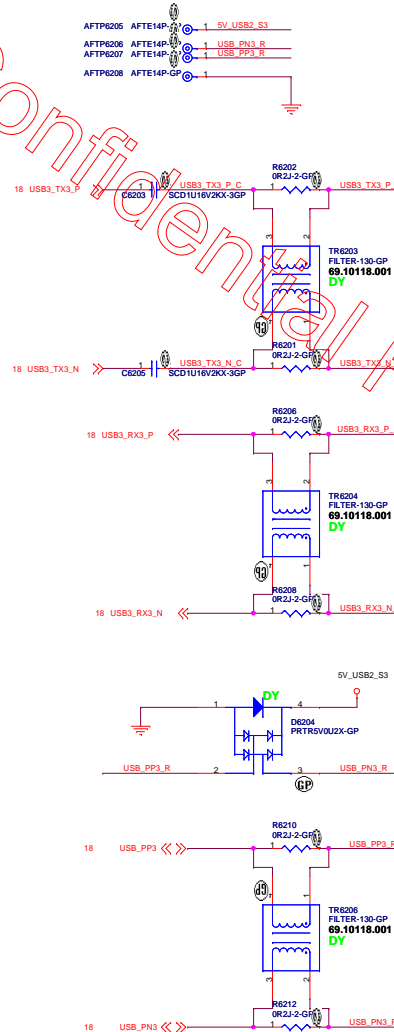
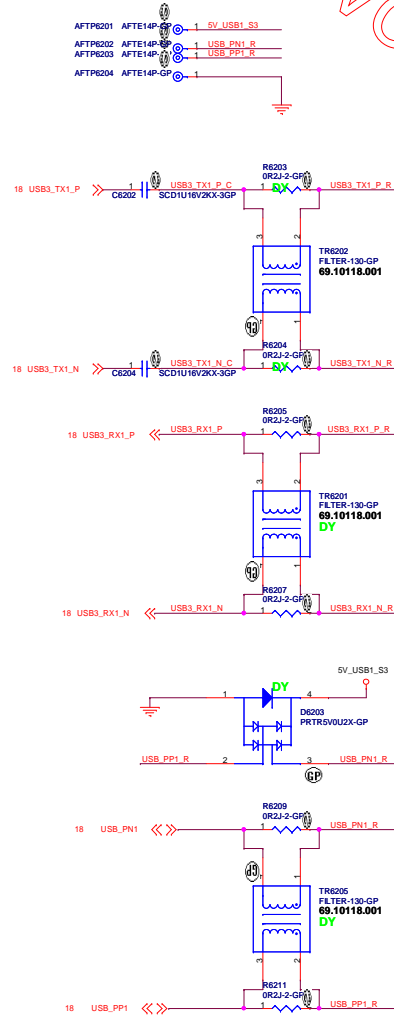
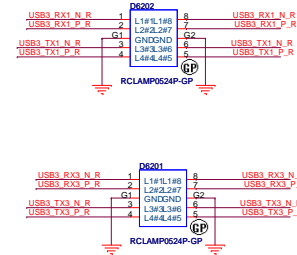
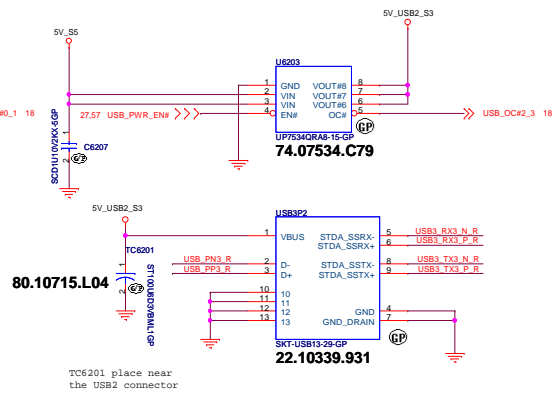
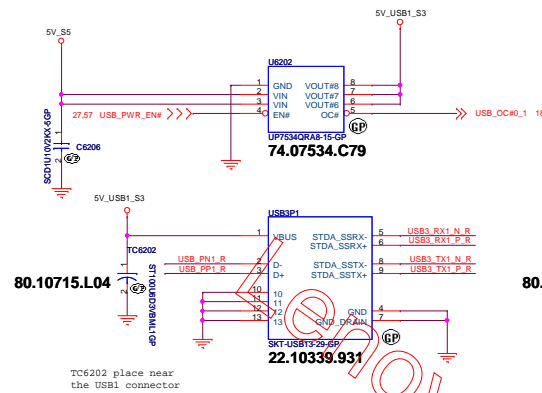
Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB Connector			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 61 of	103

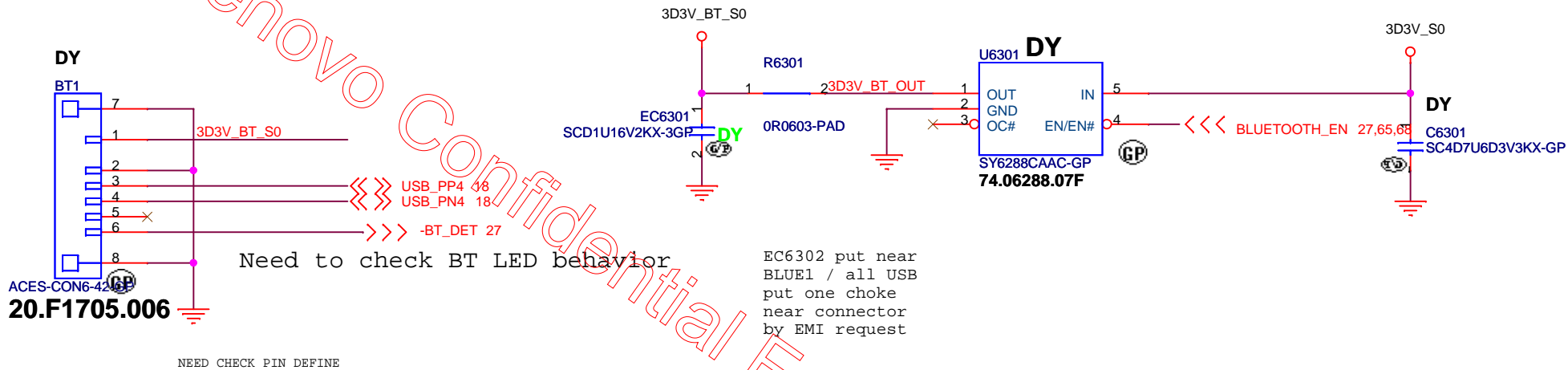
USB3.0 Port1

USB3.0 Port2

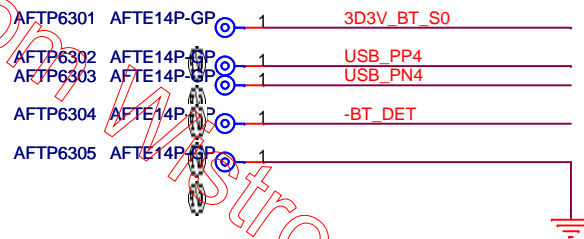


SSID = User.Interface

Bluetooth conn.



	BT CONN.	WLAN CONN.
BT1	ASM	DY
R6301	ASM	DY
U6301	ASM	DY
C6301	ASM	DY
RN1803	DY	ASM
RN1804	ASM	DY



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Bluetooth		
Size A4	Document Number LGN-1	Rev 1
Date: Wednesday, March 21, 2012		Sheet 63 of 103

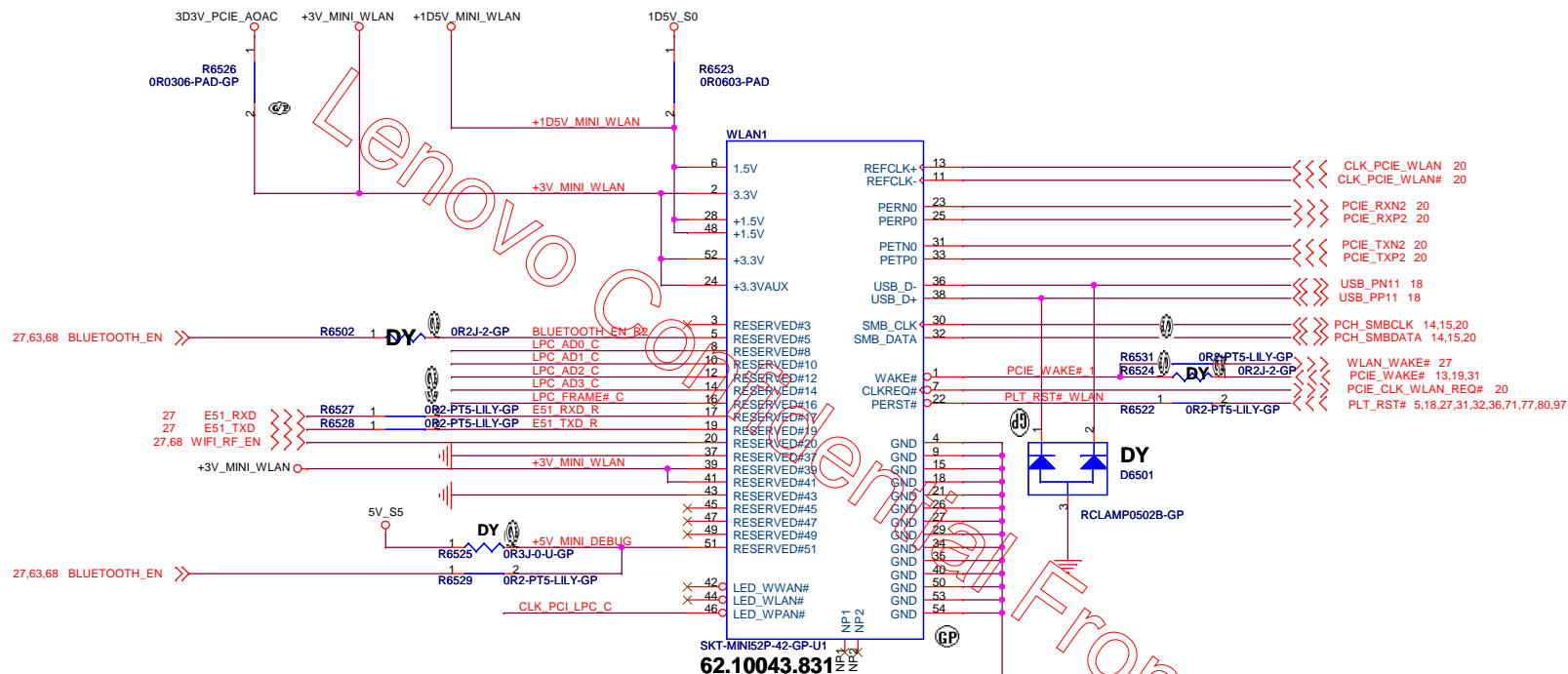
Lenovo Confidential From Wistron to PE

<Variant Name>

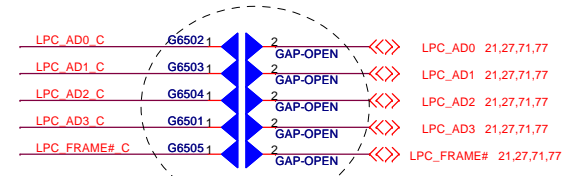
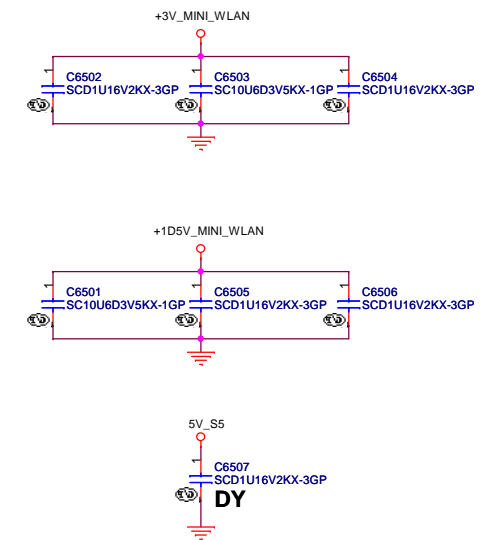
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Finger Printer Connector			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 64 of	103

SSID = Wireless

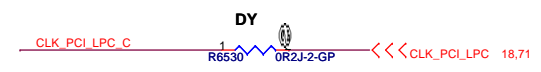
Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN

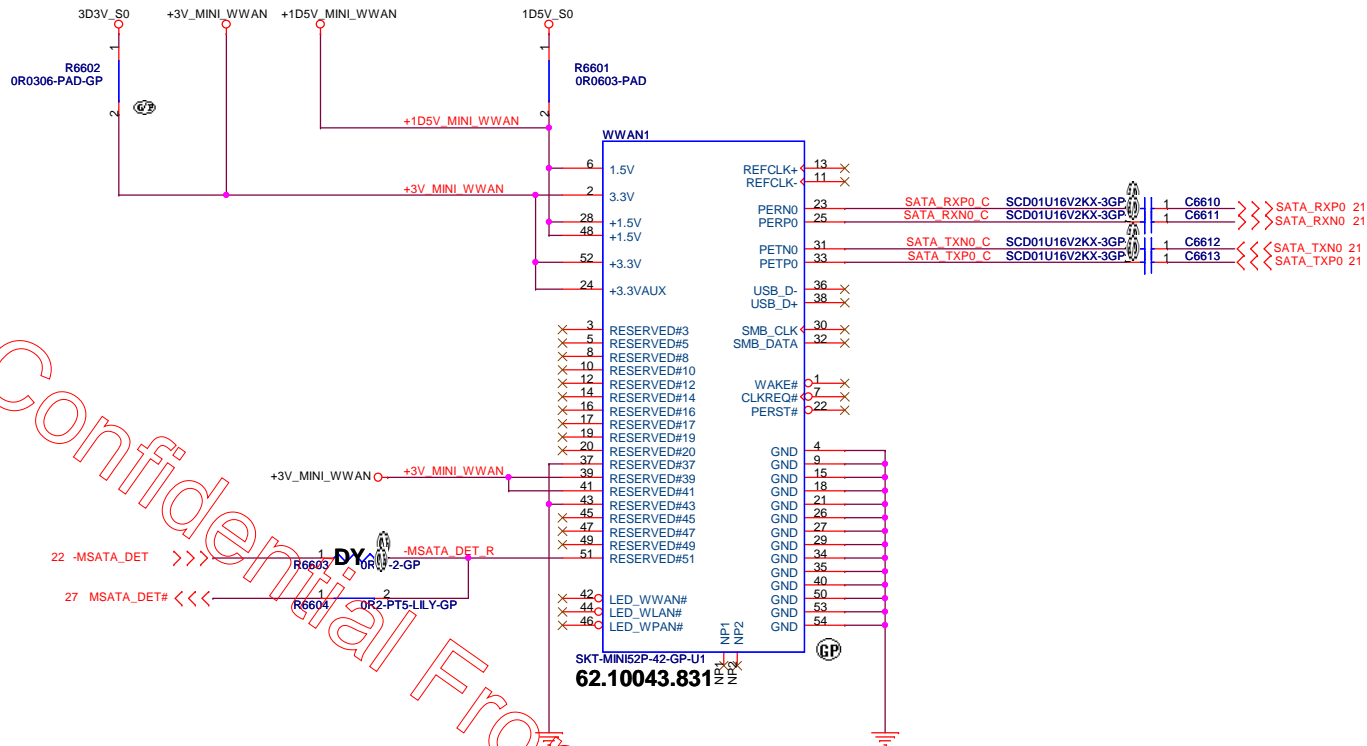
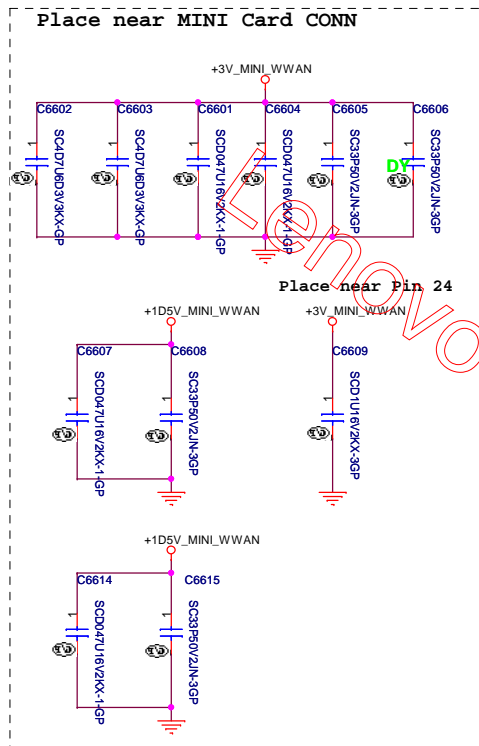


G6506~G6511
placement close close WLAN1
in bottom side



SSID = Wireless

Mini Card Connector(WWAN)



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size

Document Number

LGN-1

Rev

1

Date: Wednesday, March 21, 2012

Sheet 66 of 103

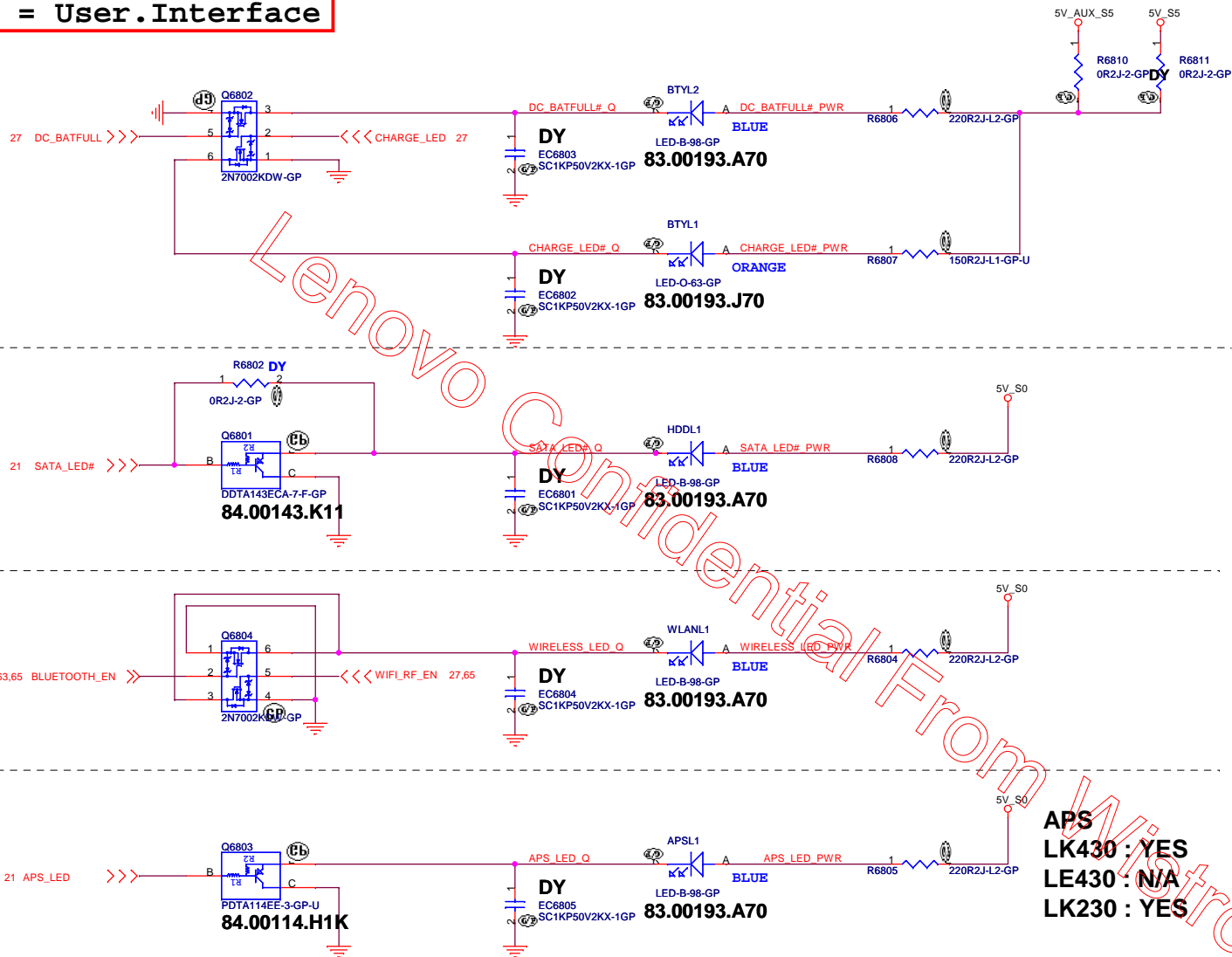
Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 67 of	103

SSID = User.Interface



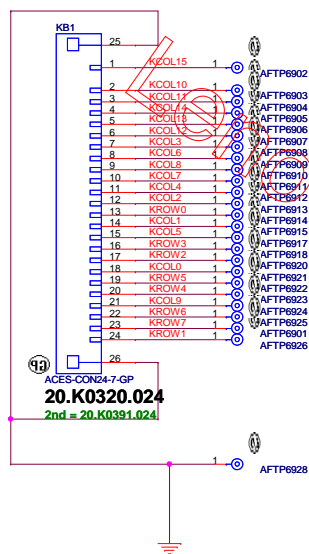
APS
LK430 : YES
LE430 : N/A
LK230 : YES

bom LA47

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title LED Bard/Power Button			
Size Custom	Document Number LGN-1	Rev 1	
Date: Wednesday, March 21, 2012	Sheet 68	of 103	

SSID = KBC

Internal KeyBoard Connector

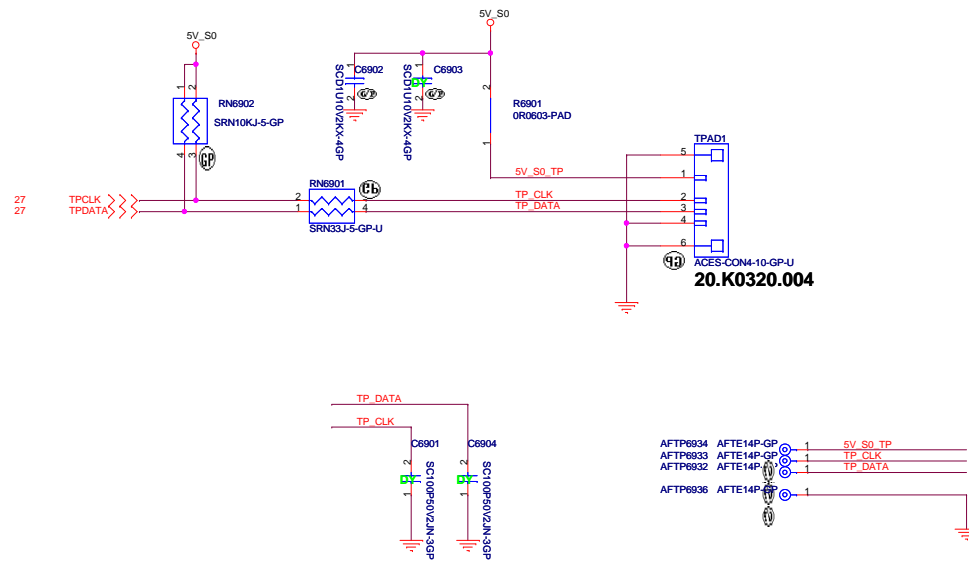


<<< KROW[0..7] 27
>>> KCOL[0..15] 27

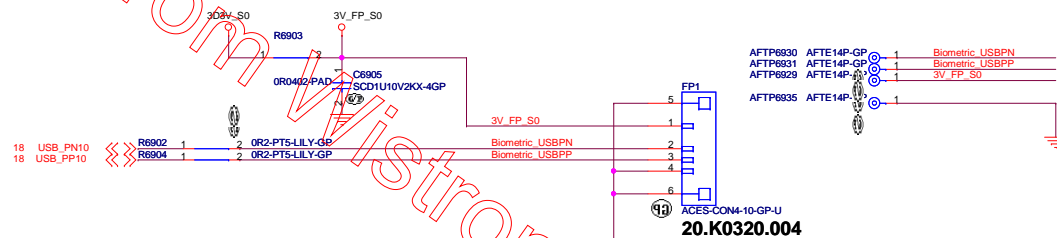
* Membrane Pin Out Top View :

PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

SSID = Touch.Pad



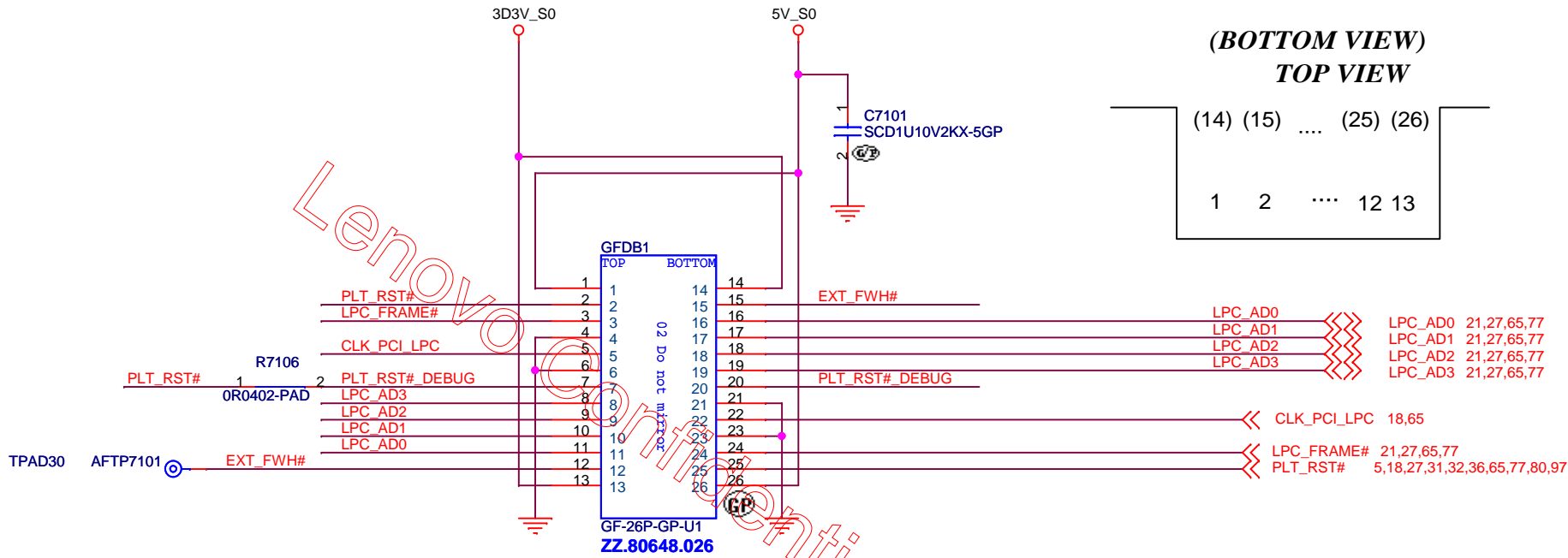
SSID = Finger Printer



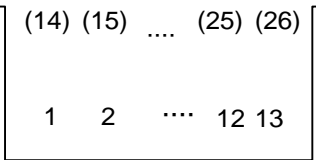
Lenovo Confidential From Wistron to PE

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Hall Sensor			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 70 of	103



(BOTTOM VIEW)
TOP VIEW



LPC_AD0 21,27,65,77
LPC_AD1 21,27,65,77
LPC_AD2 21,27,65,77
LPC_AD3 21,27,65,77
CLK_PCI_LPC 18,65
LPC_FRAME# 21,27,65,77
PLT_RST# 5,18,27,31,32,36,65,77,80,97

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Dubug connector	
Size	Document Number		Rev	
A4	LGN-1		1	
Date:	Wednesday, March 21, 2012		Sheet	71 of 103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 72 of	103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 73 of	103

Lenovo Confidential From Wistron to PE

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
New Card			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 75 of	103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

LGN-1

Rev
1

Date: Wednesday, February 15, 2012

Sheet 76 of 103

D

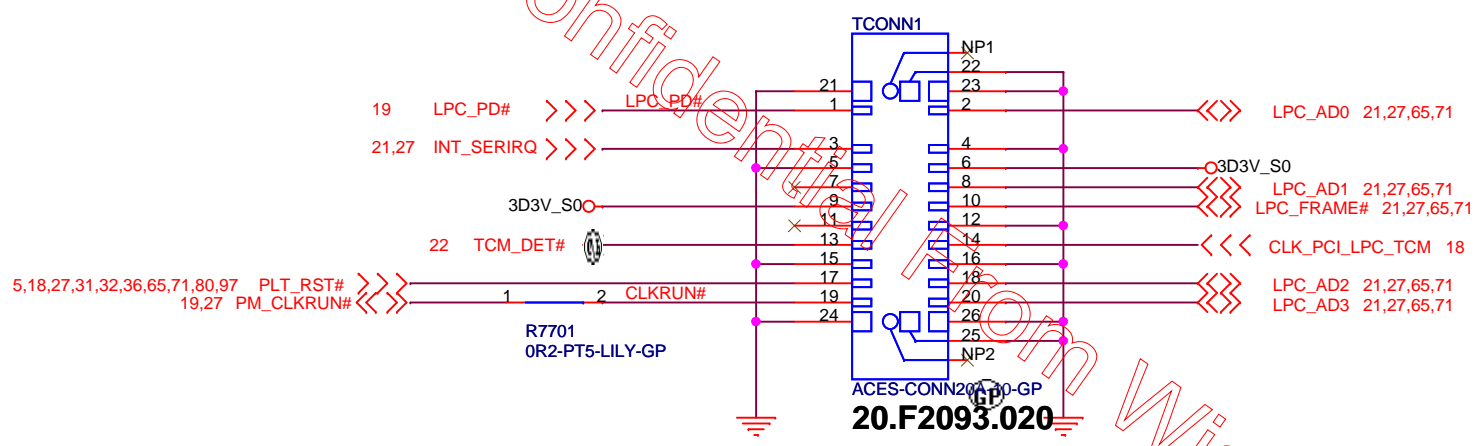
C

B

A

Lenovo Confidential Wistron to PE

TCM
LK430 : YES
LE430 : N/A
LK230 : YES



<Variant Name>

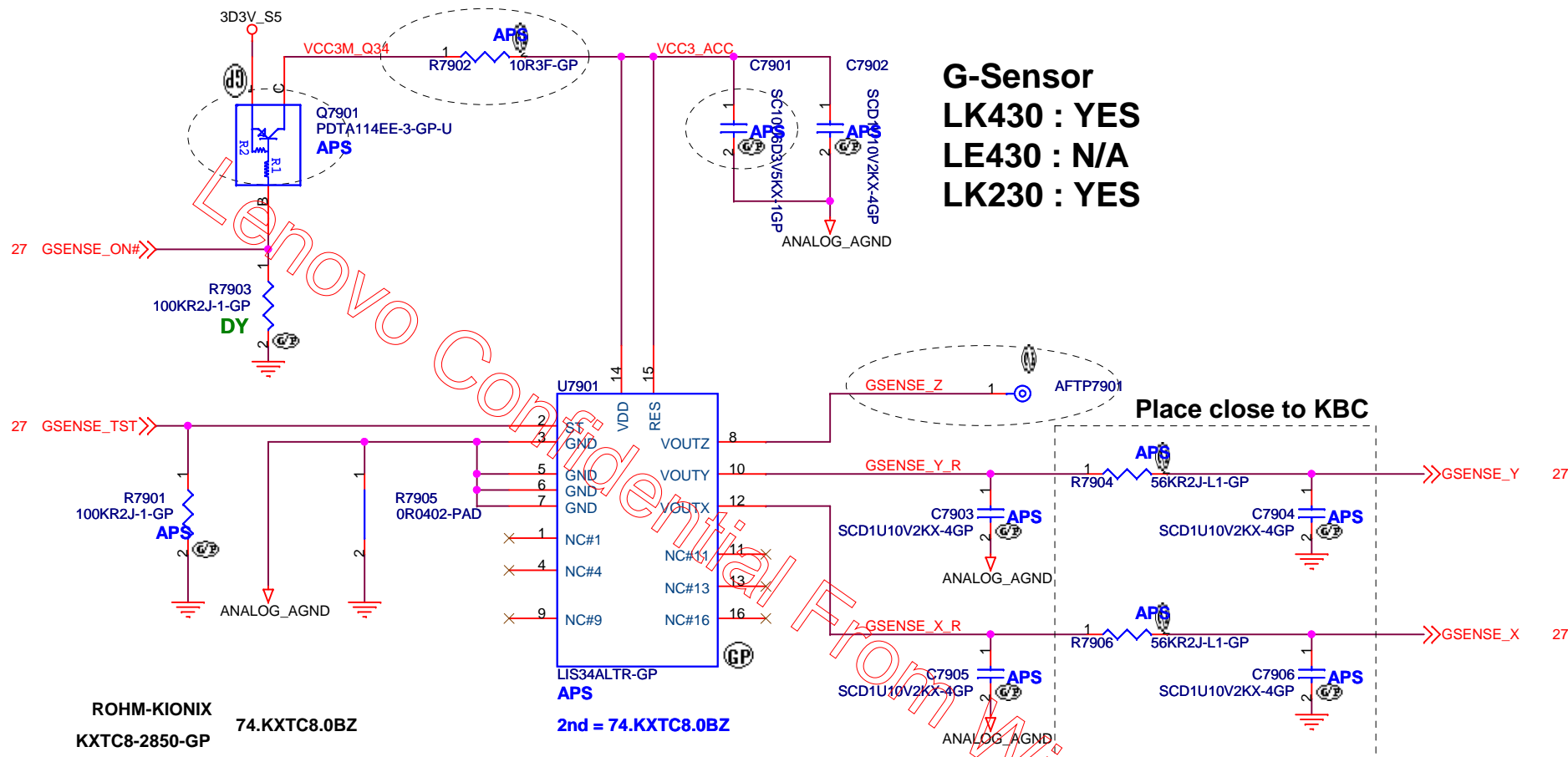
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Reserved		
Size	Document Number	Rev
A4	LGN-1	1
Date:	Wednesday, March 21, 2012	Sheet 77 of 103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

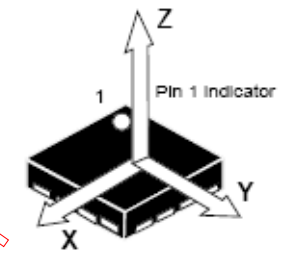
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
A4	LGN-1		1
Date: Wednesday, February 15, 2012		Sheet 78 of	103



G-Sensor
LK430 : YES
LE430 : N/A
LK230 : YES

ROHM-KIONIX
KXTC8-2850-GP
74.KXTC8.0BZ

U7901
LIS34ALTR-GP
APS
2nd = 74.KXTC8.0BZ



- Layout Comment :**
- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
 - (2) Avoid routing under DCDC switching area.

<Variant Name>

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
G-Sensor		
Size	Document Number	Rev
A4	LGN-1	1
Date:	Wednesday, March 21, 2012	Sheet 79 of 103

RFID

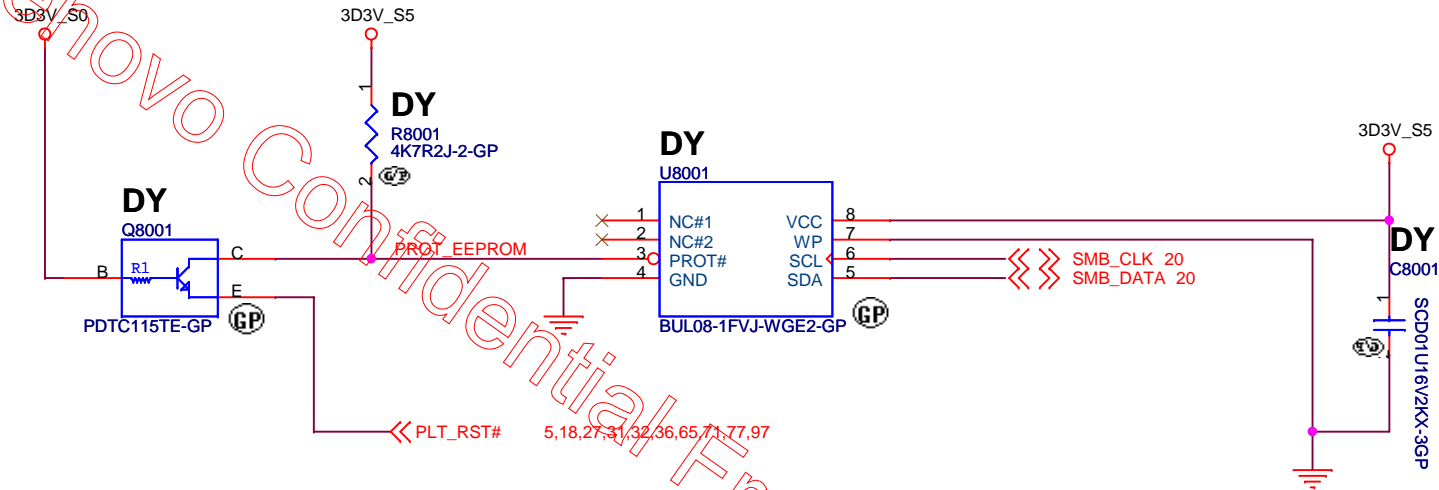


Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

LGN-1

Rev
1

Date: Wednesday, March 21, 2012

Sheet 80 of 103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

LGN-1

Rev
1

Date: Wednesday, February 15, 2012

Sheet 81 of 103



<Variant Name>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector

Size
A4

Document Number

LGN-1

Rev
1

Date: Wednesday, March 21, 2012

Sheet 82 of 103

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		N13P-NS1(1/6): PEG I/F	
Size C	Document Number		Rev 1
		LGN-1	
Date: Wednesday, February 15, 2012		Sheet 83	of 103

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
N13P-NS1(2/6): DIGITAL OUT			
Size	Document Number		Rev
C	LGN-1		1
Date:	Wednesday, February 15, 2012		Sheet 84 of 103

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taippei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taippei Hsien 221, Taiwan, R.O.C.	
Title N13P-NS1(3/6): VRAM I/F			
Size C	Document Number LGN-1	Rev 1	
Date: Wednesday, February 15, 2012		Sheet 85 of 103	

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
N13P-NS1(4/6): GPIO			
Size	Document Number		Rev
C	LGN-1		1
Date:	Wednesday, February 15, 2012	Sheet 86 of	103

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		N13P-NS1(5/6): POWER	
Size C	Document Number		Rev 1
		LGN-1	
Date: Wednesday, February 15, 2012		Sheet 87 of	103

Lenovo Confidential From Wistron to PEG

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **N13P-NS1(6/6): GND**

Size B	Document Number LGN-1	Rev 1
-----------	---------------------------------	-----------------

Date: Wednesday, February 15, 2012	Sheet 88 of 103
------------------------------------	-----------------

Lenovo Confidential From Wistron to PE

«Core Design»		
緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia,		
Taipei 10611, Taiwan, R.O.C.		
Title VRAM CHANNEL-A		
Size A2	Document Number LGN-1	Rev 1
Date: Wednesday, February 15, 2012 Sheet 89 of 103		

Lenovo Confidential From Wistron to PE

<Core Design>		
<div>緯創資通 Wistron Corporation</div> <div>21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title VRAM CHANNEL-B		
Size A2	Document Number LGN-1	Rev 1
Date: Wednesday, February 15, 2012 Sheet 90 of 103		

Lenovo Confidential From Wistron to PE

<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title VIDEO MEMORY TERMINATION			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 91 of	103

Lenovo Confidential From Wistron to PE

JV10-CS

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: TPS51728_VGA_CORE			
Size	Document Number	LGN-1	Rev 1
Date: Wednesday, February 15, 2012		Sheet	92 of 103

Lenovo Confidential From Wistron to PE

JV10-CS

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DISCRETE VGA POWER			
Size A3	Document Number	LGN-1	Rev 1
Date: Wednesday, February 15, 2012		Sheet 93 of	103

D

C

B

A

BLANK

Lenovo Confidential From Wistron to PE

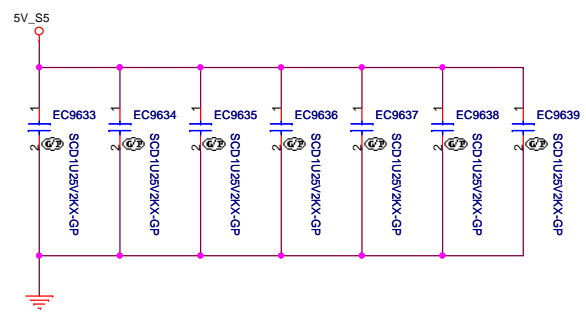
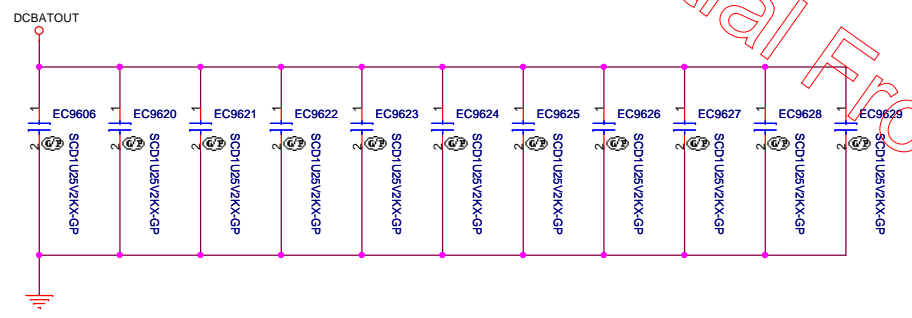
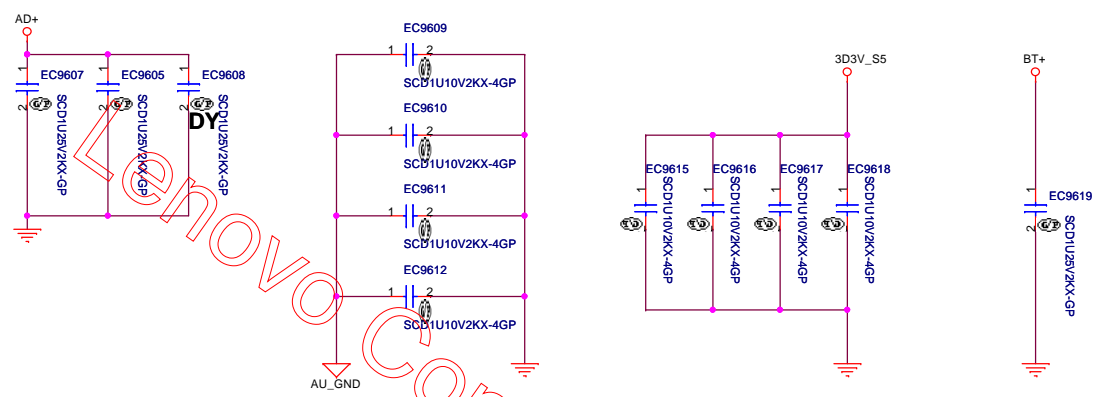
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</div>		
Title <Title>		
Size A4	Document Number LGN-1	Rev 1
Date:	Wednesday, February 15, 2012	Sheet 94 of 103

Lenovo Confidential From Wistron to PE

BLANK

<Variant Name>

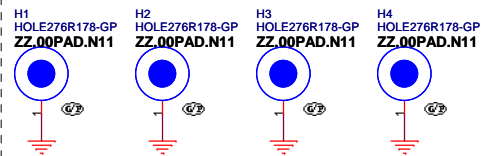
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number LGN-1		Rev 1
Date: Wednesday, February 15, 2012		Sheet 95 of	103



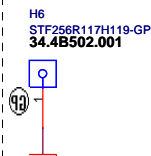
<Variant Name>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
EMI Capacitors			
Size A3	Document Number LGN-1		Rev 1
Date:	Wednesday, February 15, 2012	Sheet 96 of	103

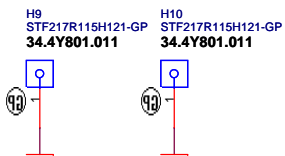
CPU Plate



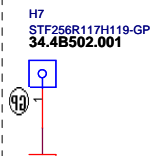
MiniPCI Std-off



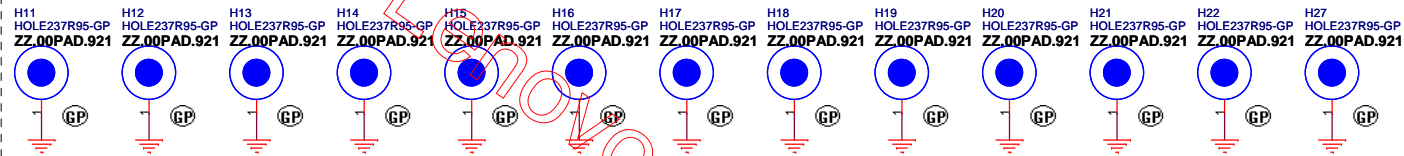
PCH Std-off



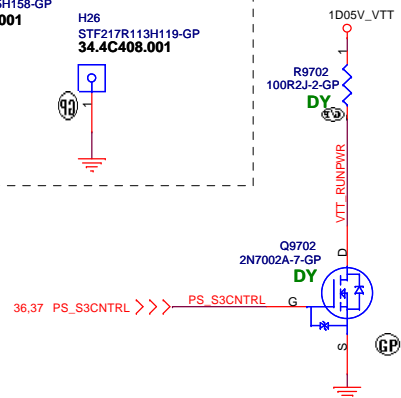
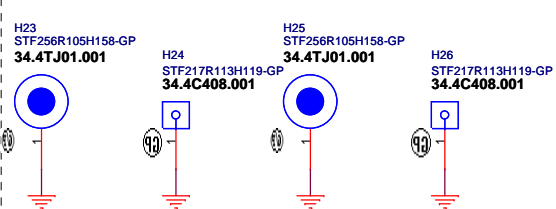
SSD STD-OFF



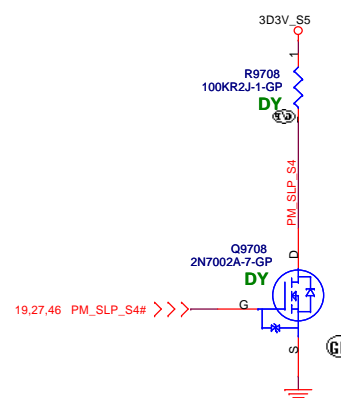
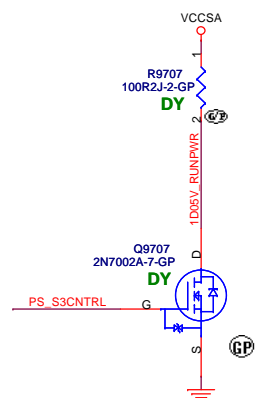
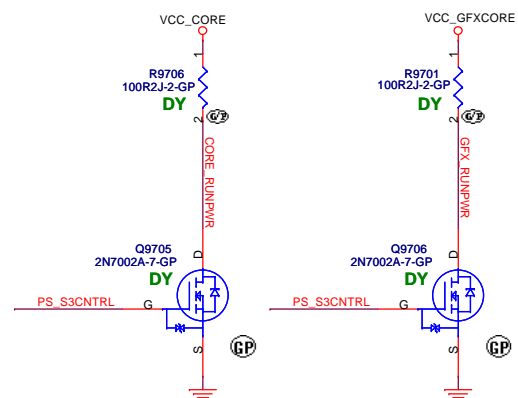
Structure boss



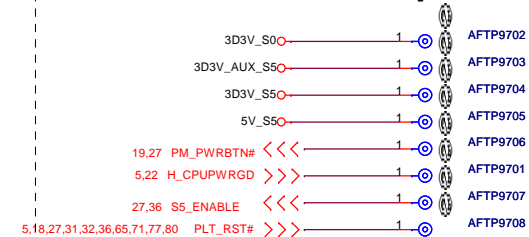
Structure boss



For Discharge



Check test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

緯創資通

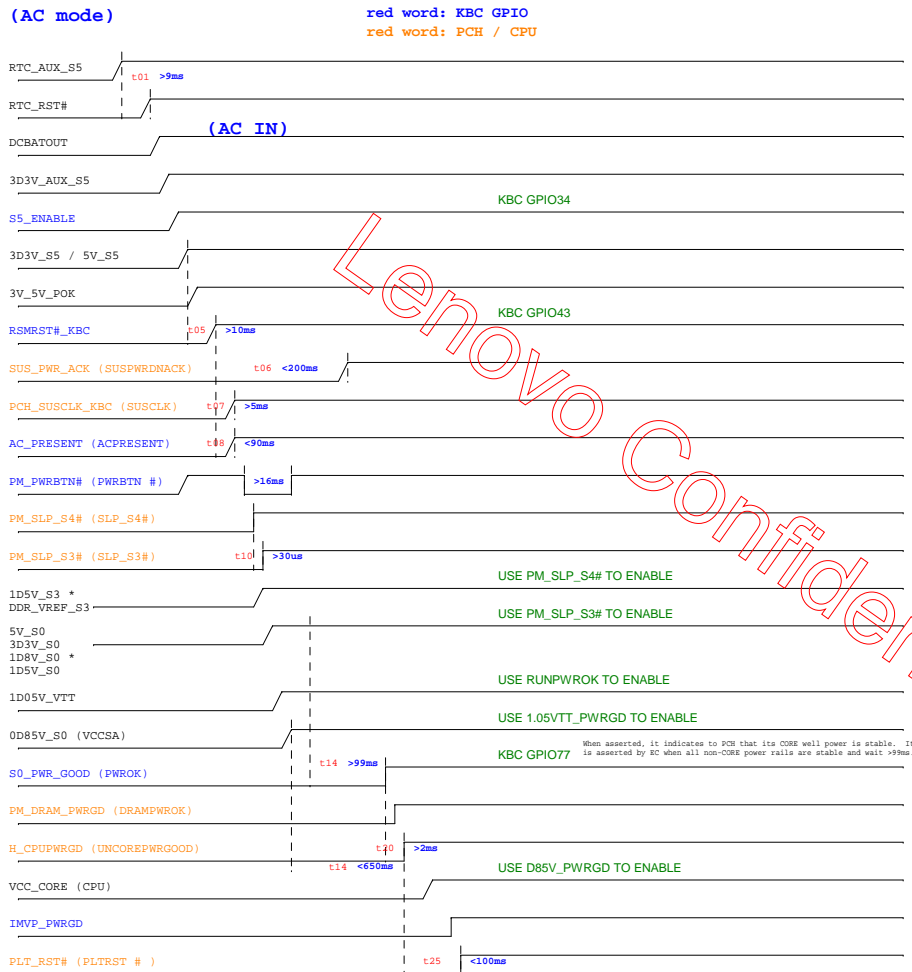
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

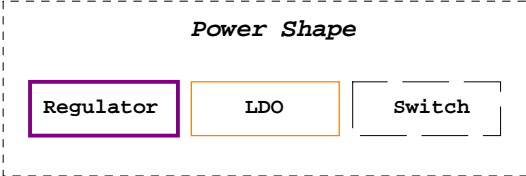
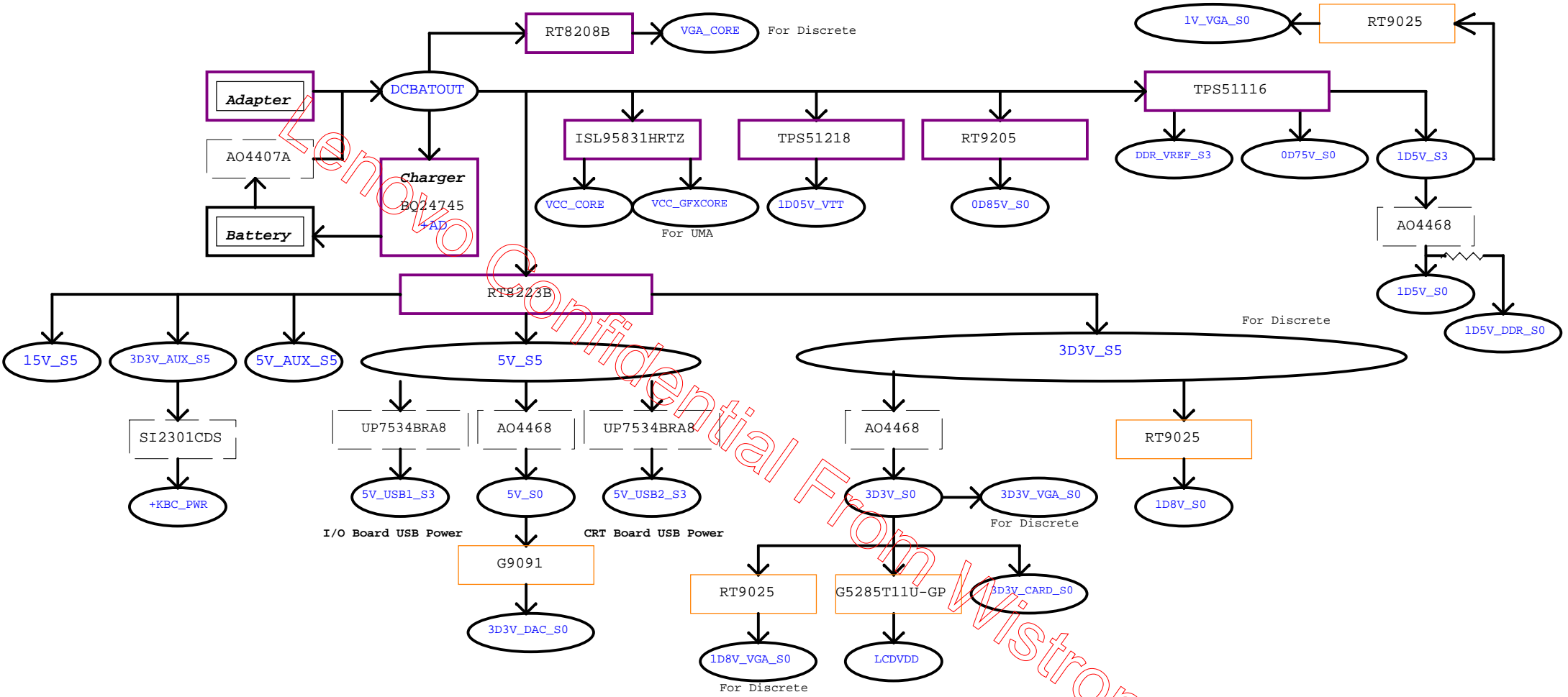
Title		
UNUSED PARTS/HOLES/GND/PADS		
Size	Document Number	Rev
A3	LGN-1	1
Date: Wednesday, March 21, 2012		
Sheet 97 of 103		

Lenovo Confidential From Wistron to PE

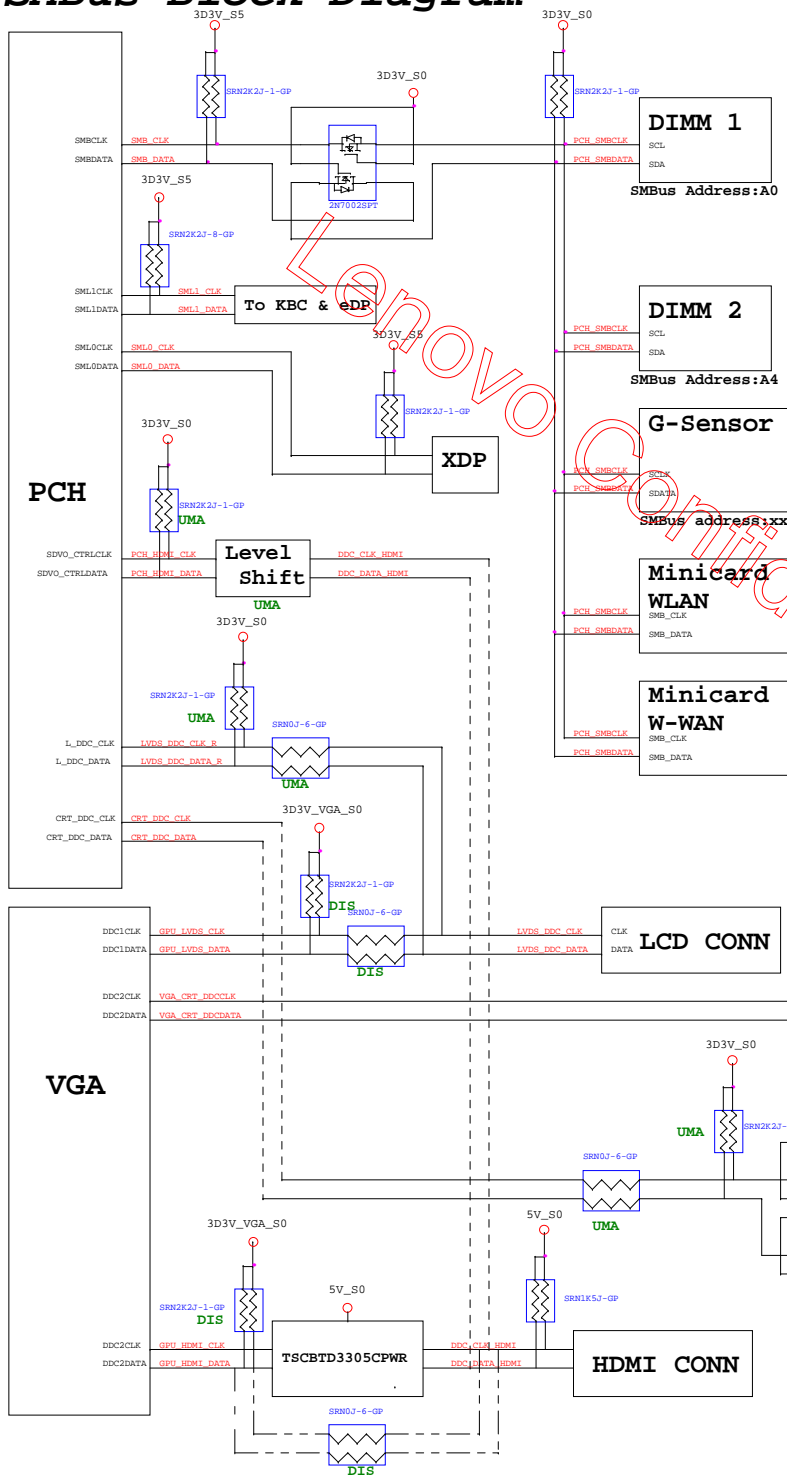
(Blanking)

<Variant Name>		
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Change History		
Size A4	Document Number LGN-1	Rev 1
Date: Wednesday, February 15, 2012		Sheet 98 of 103

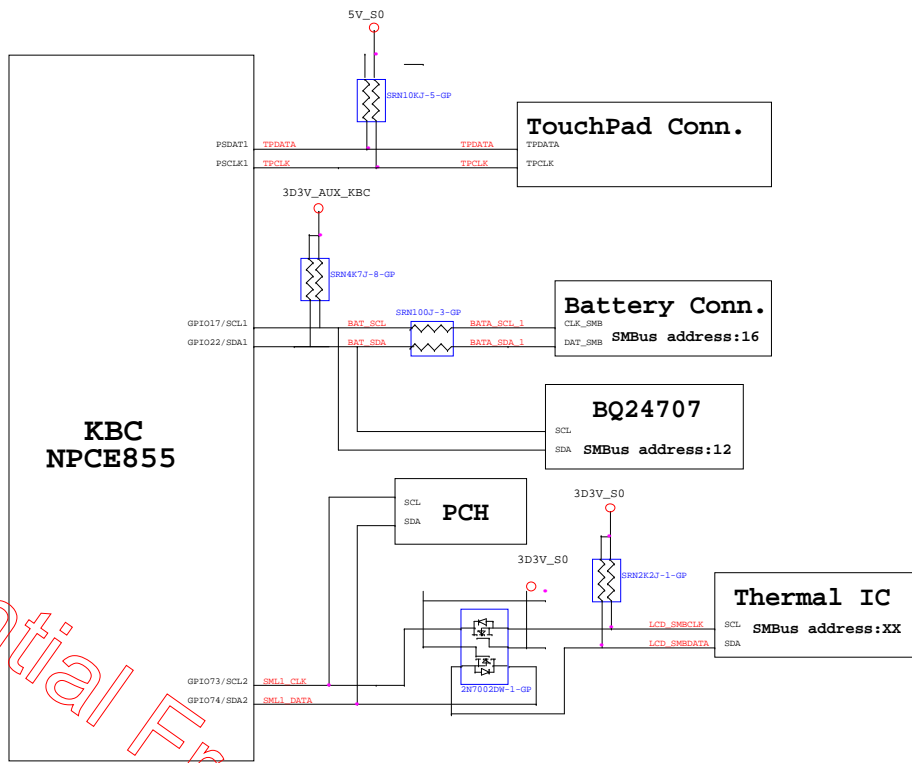




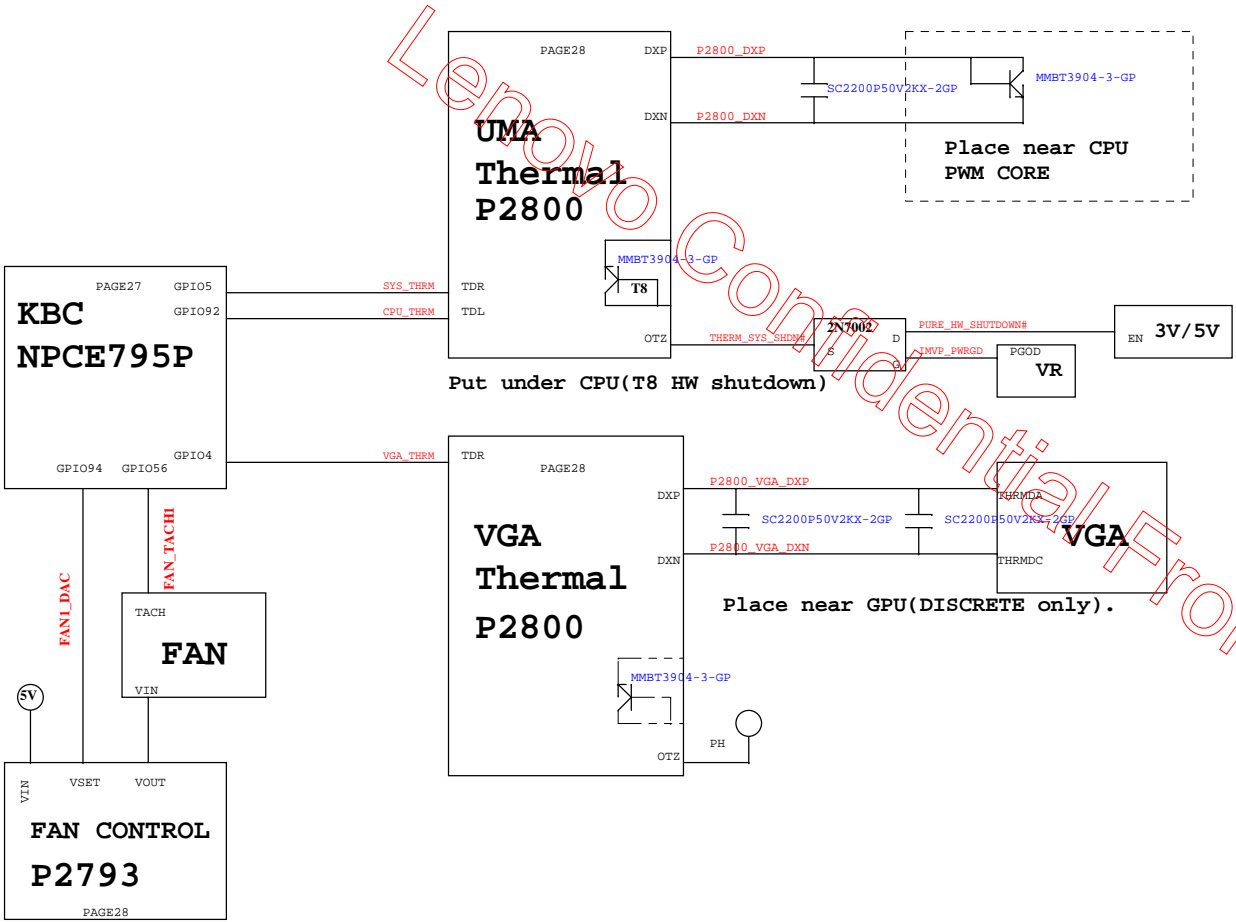
PCH SMBus Block Diagram



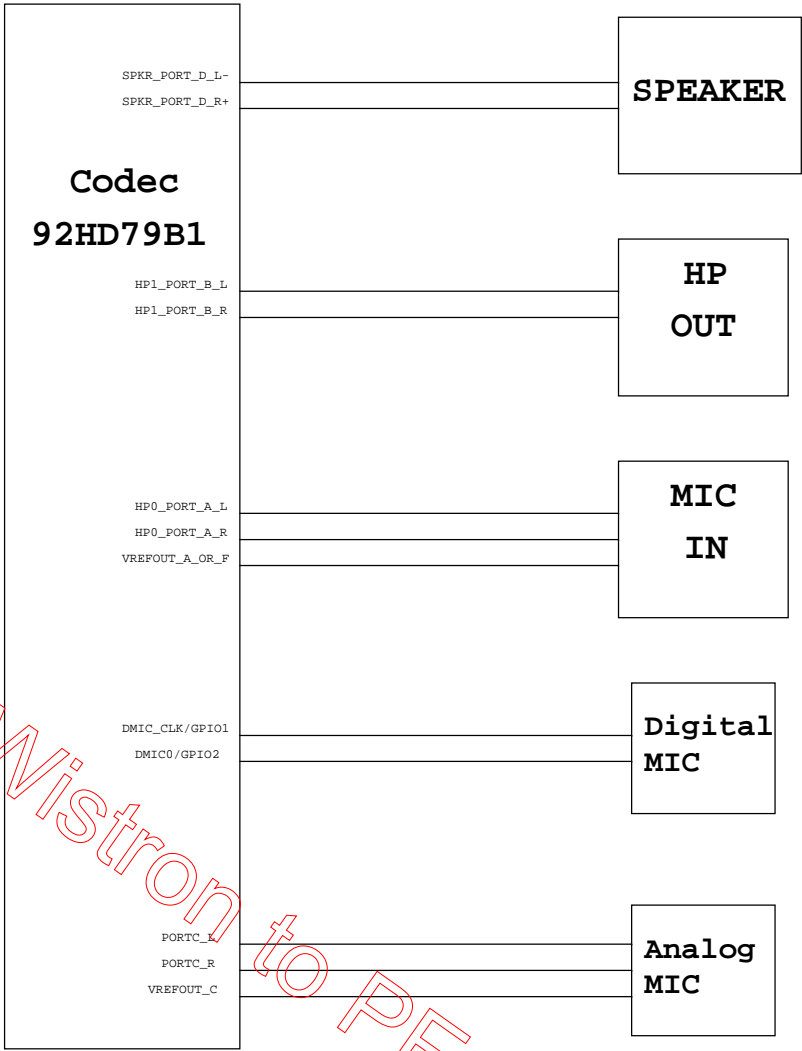
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Lenovo Confidential From Wistron to PE

(Blanking)

<Variant Name>		
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Change History		
Size A4	Document Number LGN-1	Rev 1
Date: Wednesday, February 15, 2012		Sheet 103 of 103